MEMS Packaging

ESS4810 Lecture
Fall 2010

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- Microsystems Packaging
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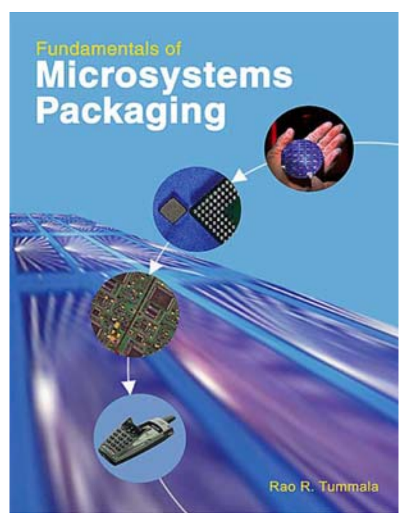
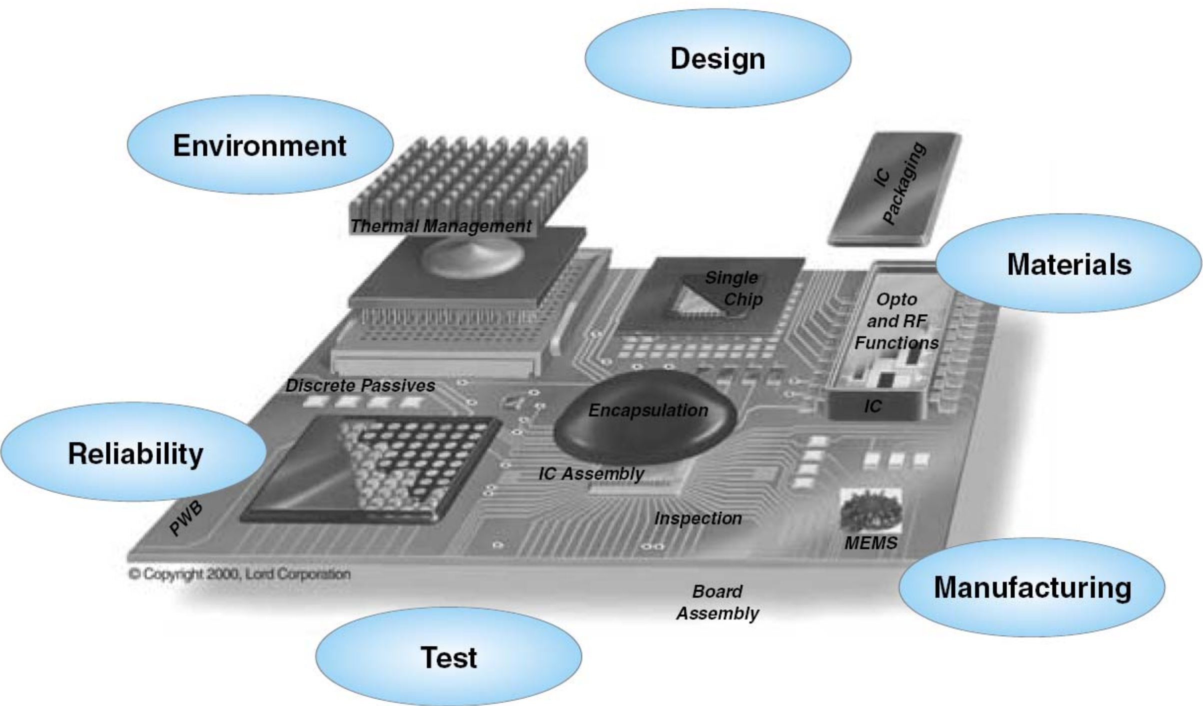
- Bonding
- MEMS Packaging



Microsystems Packaging

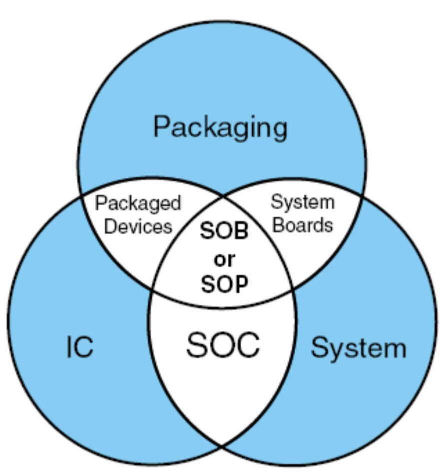
- A $125 billion worldwide market, employing more than a million people
- Miniaturized and integrated systems
  - Microelectronics, Photonics, MEMS and RF Devices
  - Systems Engineering
  - Systems Packaging
- Packaging is defined as the bridge that interconnects the ICs and other components into a system to form electronic products

Microsystems Packaging



Integration

- System-on-Board (SOB): a number of packaged ICs and other components assembled onto a system-level board
- System-on-Chip (SOC)
- System-on-Package (SOP), or System-in-Package (SIP) is analogous to SOC, in that it is a single component, multi-function, multi-chip package providing all the needed system-level functions
- Both SOC and SOP are expected to be the wave of the future.

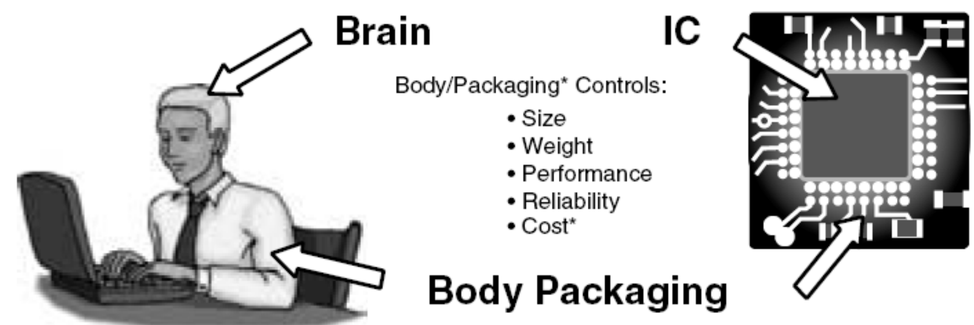


IC and MEMS Packaging

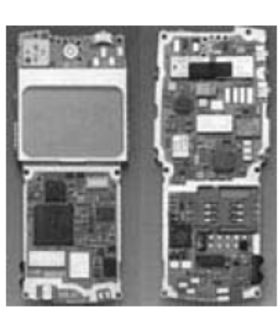
- **IC Packaging**
  - **The approximate IC fabrication cost, excluding design cost, is about $\$4/cm^2$ at mature production levels**
  - **Well-developed (dicing, wire bonding, …)**
  - **30% to 95% of the whole manufacturing cost**
- **MEMS Packaging**
  - **Specially designed packaging processes**
  - **Difficult due to moving structures, chemicals …**
  - **The most expensive process in micro-fabrication**

Electronics Packaging

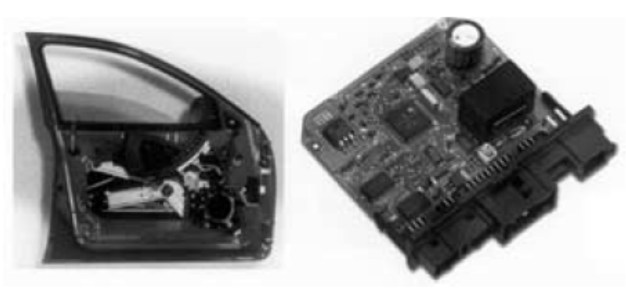
- Electronics have to be packaged
- Functions:
  - Protecting, powering, and cooling
  - Electrical and mechanical connection/ interface
- Challenge:
  - Providing all crucial functions required **without limiting the performance**



(a) Inside a Computer



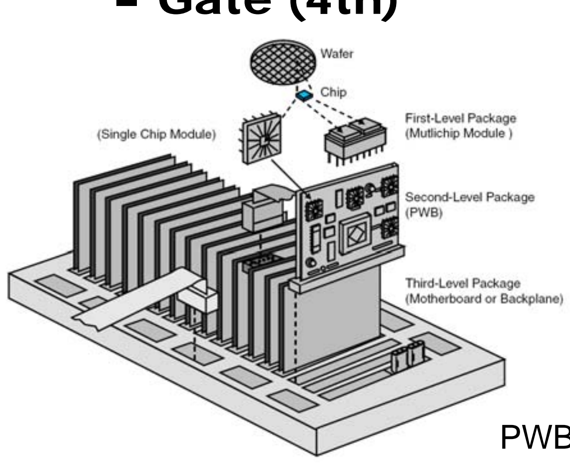
(b) Inside a Cellular Phone

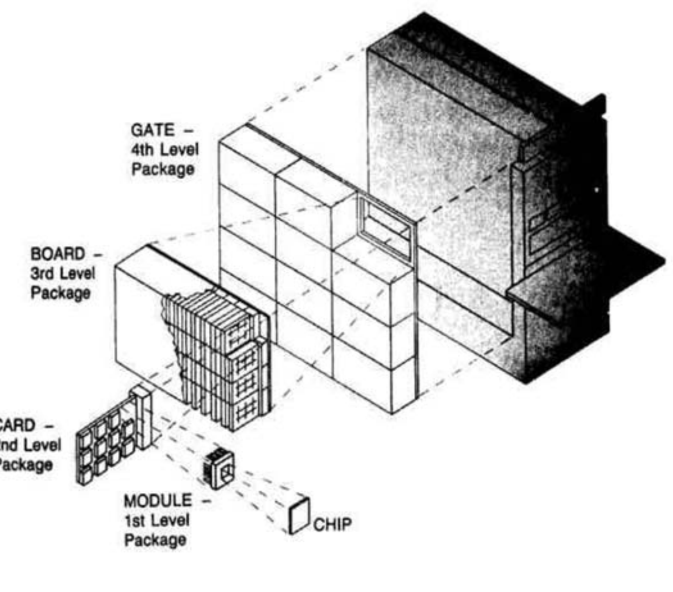


(c) Inside an Automobile

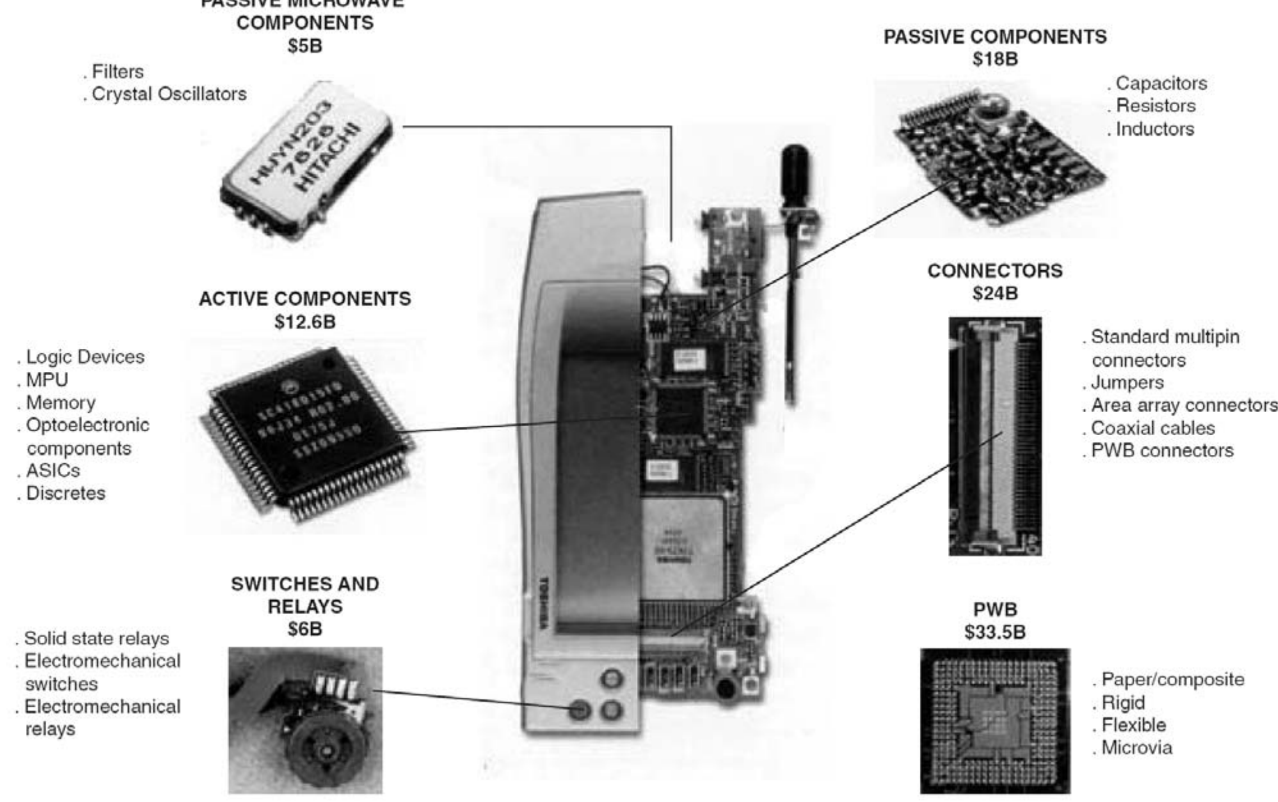
Electronics Packaging

- **Package hierarchy**
  - **Chip**
  - **Module (1st)**
  - **Card (2nd)**
  - **Board (3rd)**
  - **Gate (4th)**

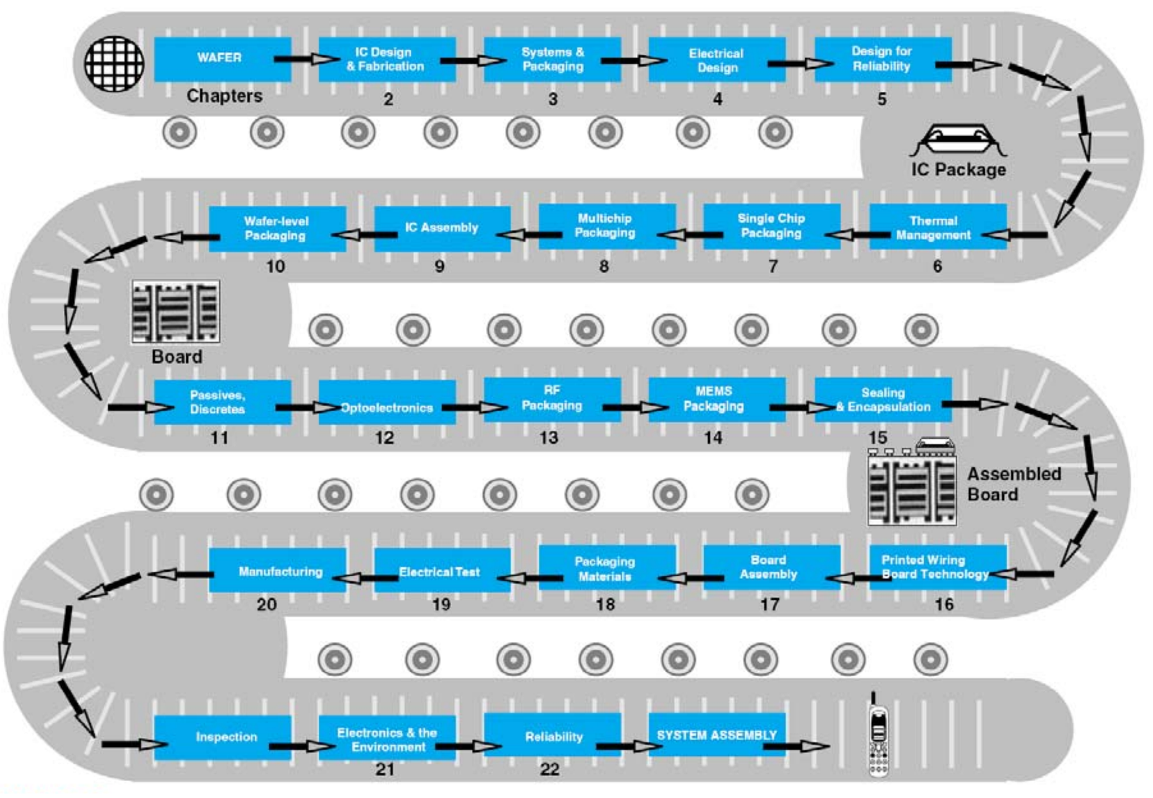




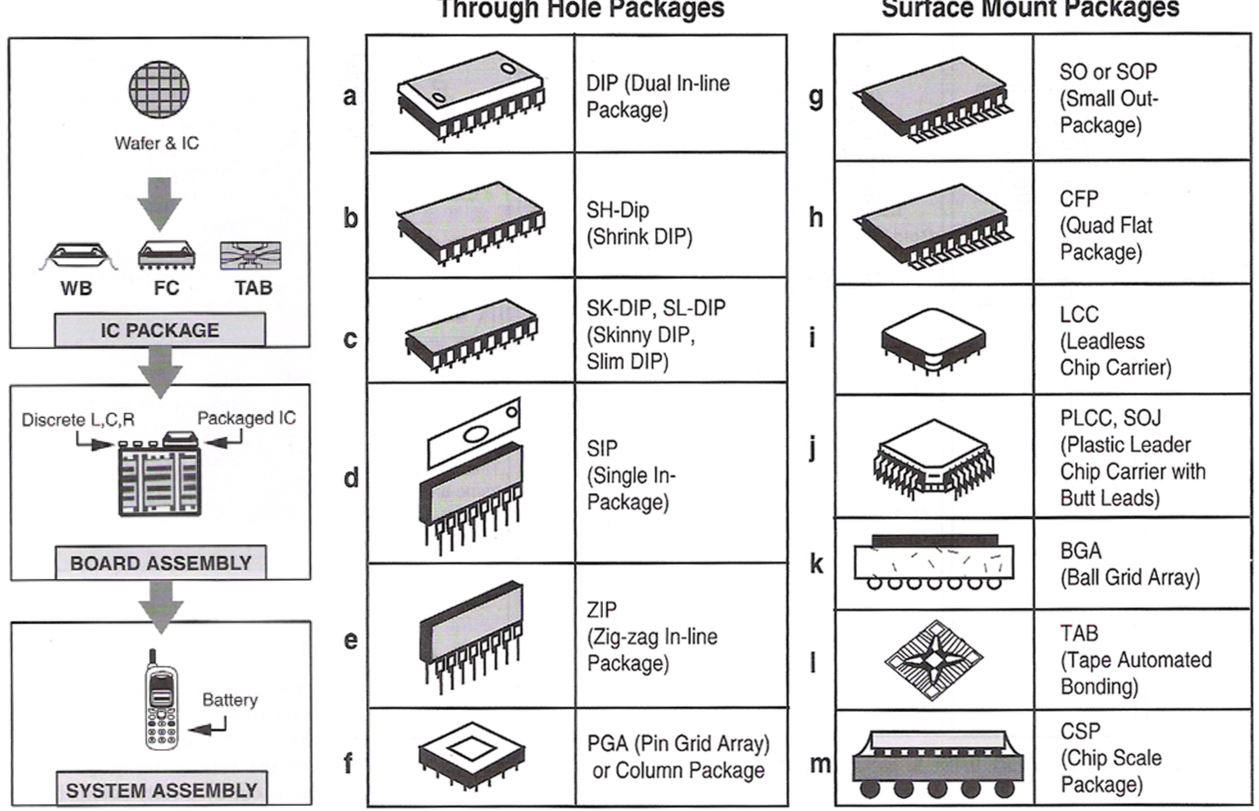
PWB: printed wiring board



Critical Microsystem Packaging Technologies from Wafer to System-Level Board



IC Packaging



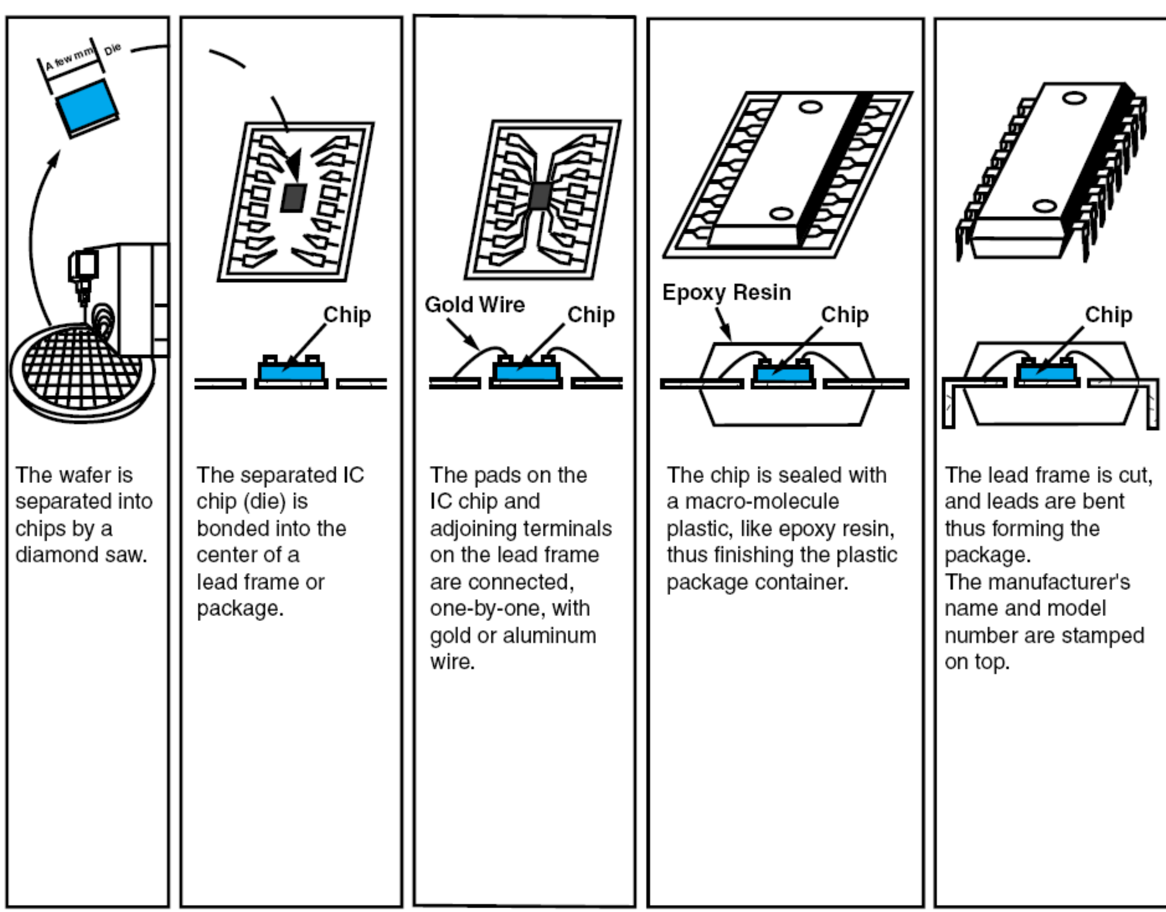
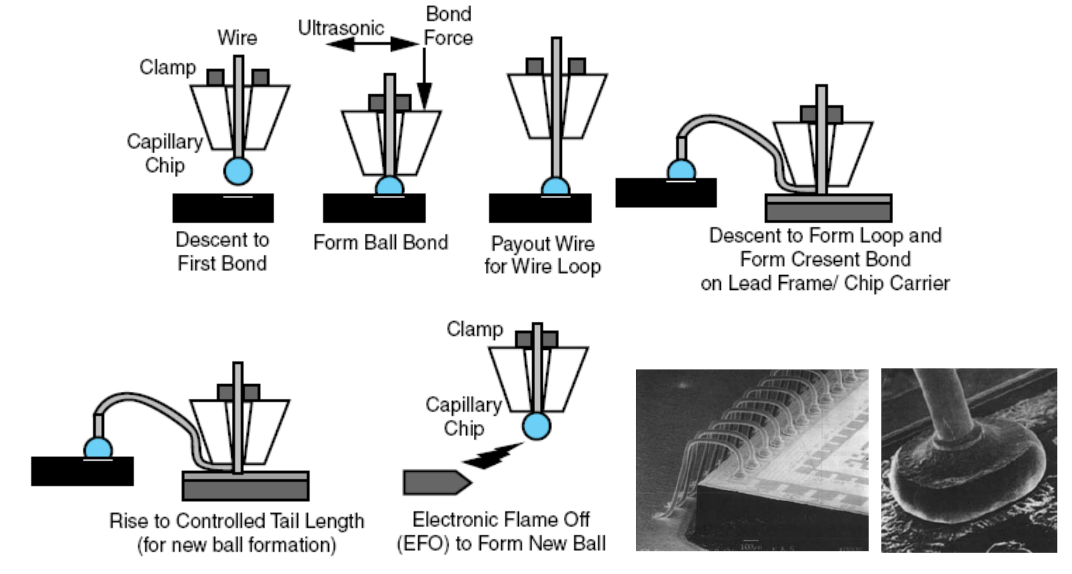


FIGURE 2.22 An example of dual in-line IC packaging with wirebonding.

WireBonding

- **A chip-to-package interconnection technique where a fine metal wire is attached between each of the I/O pads on the chip and its associated package pin, one at a time**



Wafer Level Packaging

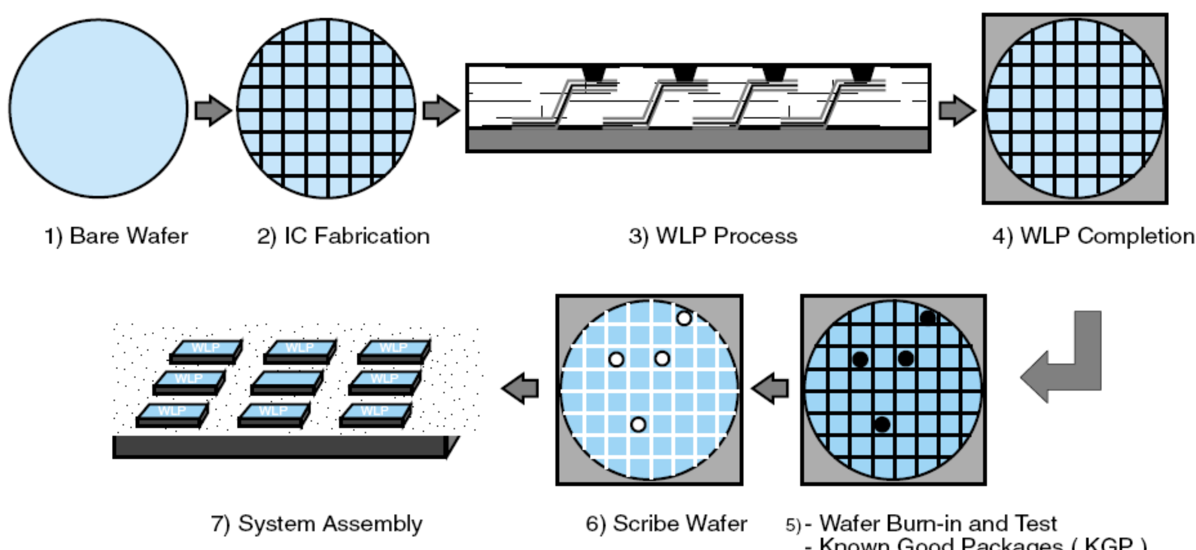
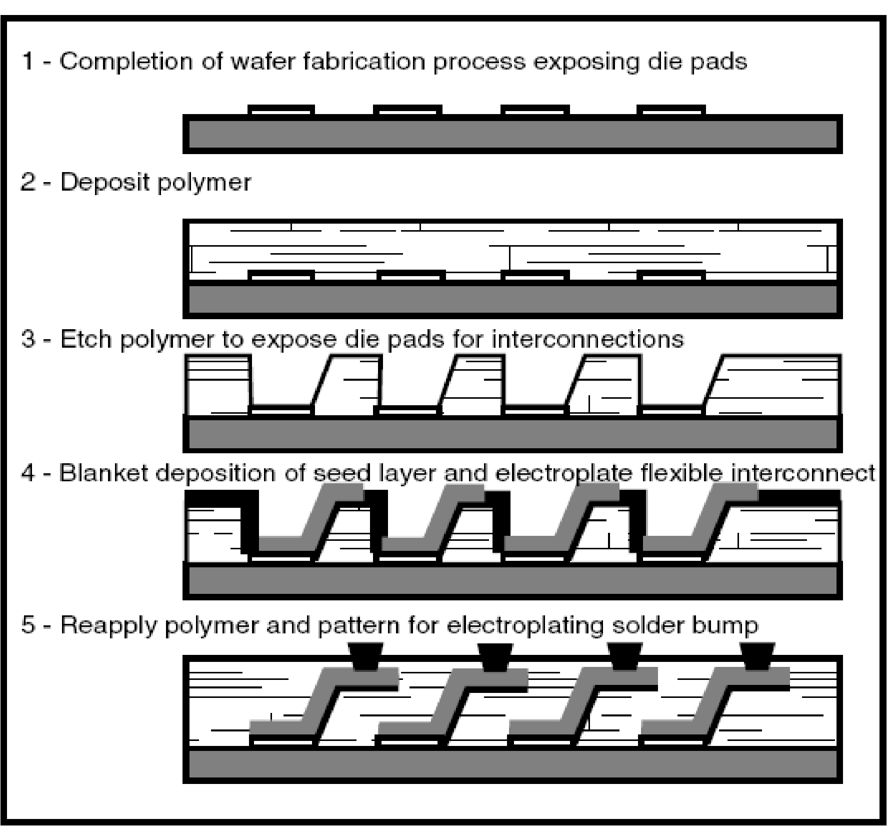
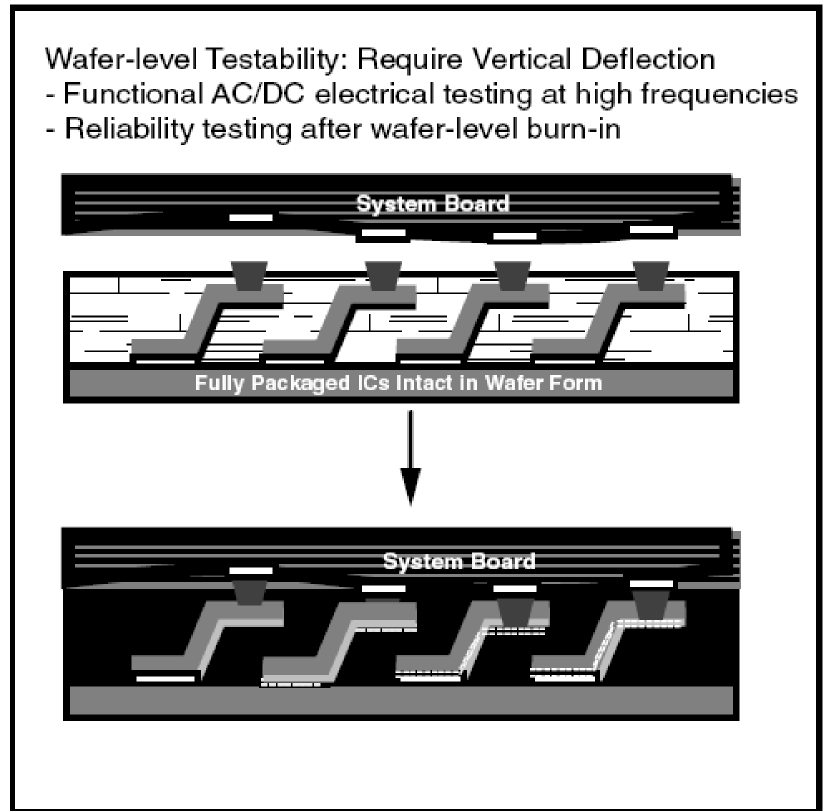


FIGURE 10.8 An example of a complete wafer-level packaging process. (*Courtesy of IFC, Georgia Tech*)

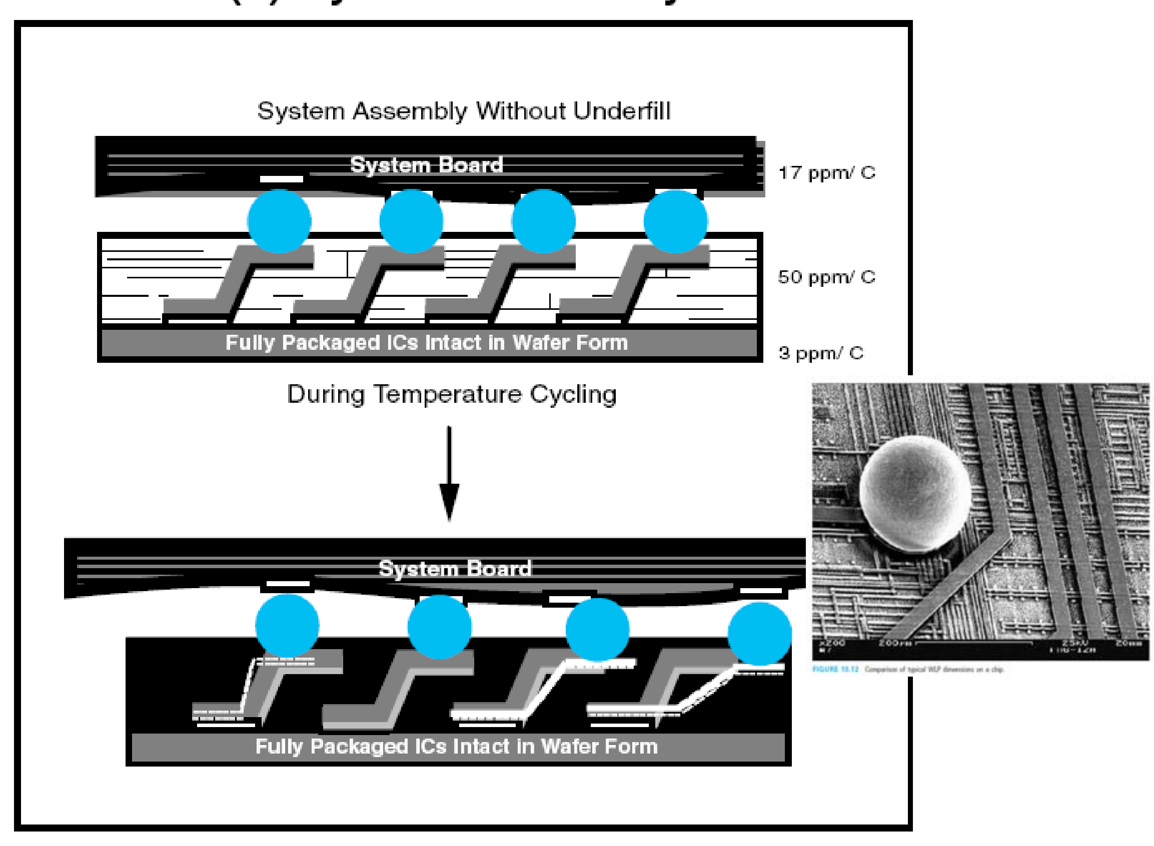
(a) Fabrication Process



(b) Testing



(c) System Assembly



Bonding

- Permanently seal solid-state materials with smooth and flat surfaces, most often by chemical reactions
  - Allow the fabrication of multi-layer, sandwiched, micromechanical structures, in which each layer can contain three-dimensional structures
  - Allow the multi-chip production of microsystems with many micromechanical structures and/or microelectronic structures bonded to the single silicon or glass substrate platform
  - Very good techniques for packaging of microsystems

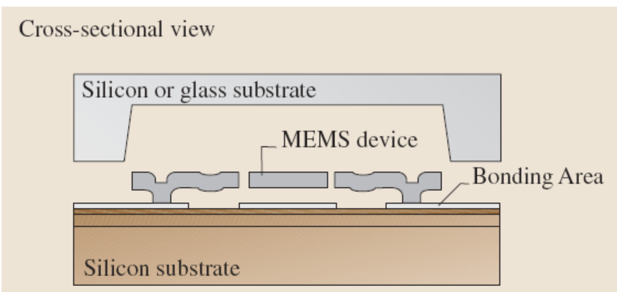
Basic Requirements

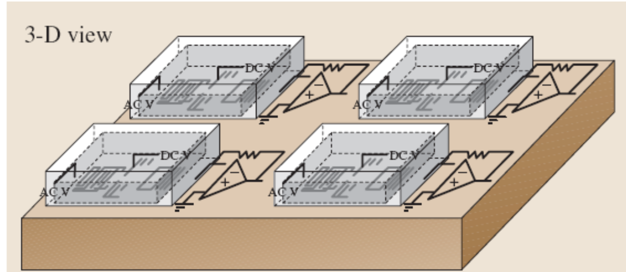
- Surface cleanliness
  - Particles trapped between wafers can lead to the formation of voids and failure of the bond
- Minimal process-induced stress
  - Thermal mismatch
- Stable and strong
- Strain relief

Bonding

- Carried out in the range of high (>700°C), medium (200~500°C) or low temperatures (20~200°C)

- Fusion bonding
- Anodic (electrostatic) bonding
- Eutectic bonding
- Adhesive bonding





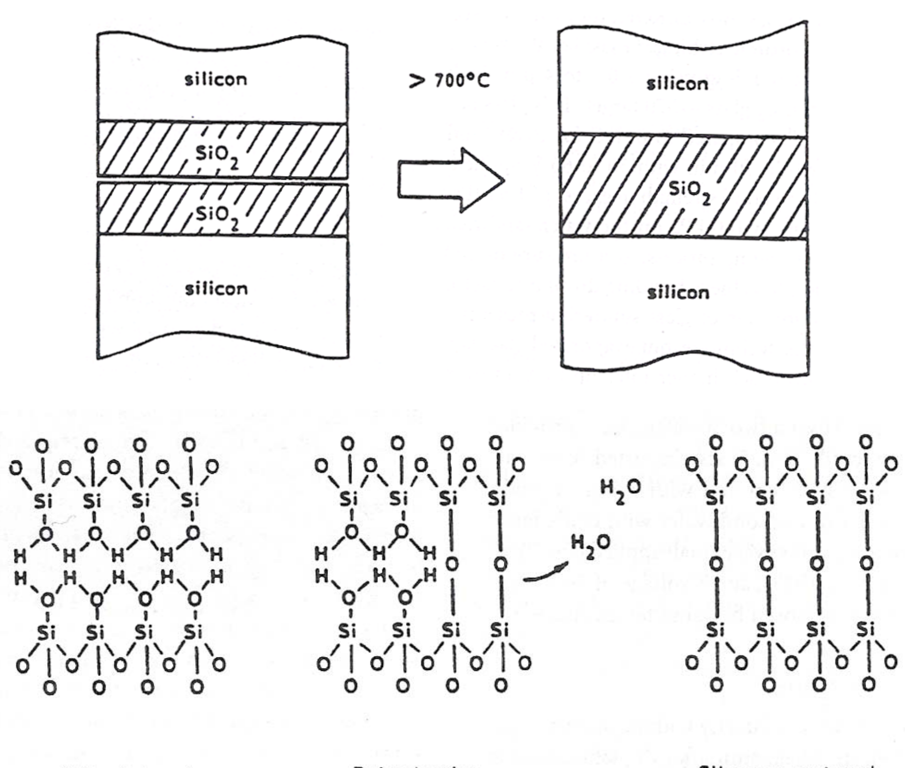
Fusion Bonding

- Joining silicon to silicon
  - Placing the surfaces in close contact, inserting them in an oxidizing ambient at temperatures > 800°C (not IC compatible), and then annealing
- Quality
  - Depending critically on temperature (> 1000°C) and roughness (< 4 nm)
  - Strength up to 20 MPa

Fusion Bonding

- Chemical reaction between OH-groups (native or grown oxide)
- Wafers must undergo hydration to create hydrophilic top layer consisting O-H bonds
- Bonding systems
  - Si + Oxidized Si wafer
  - two Oxidized Si wafer
  - two bare Si wafers
  - Si + Si with a thin layer (< 200 nm) nitride

Bonding Mechanism

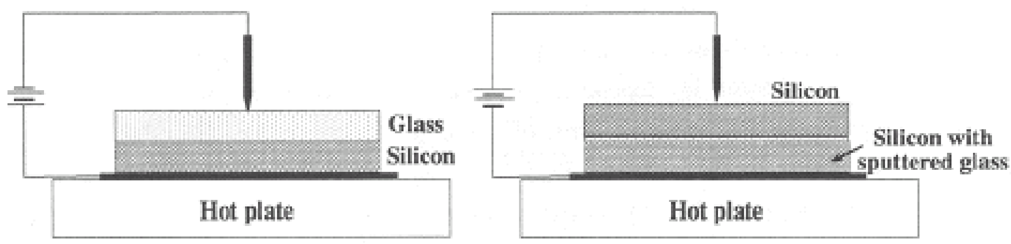


Fusion Bonding

- Bond strength after various annealing temperatures
- < 300°C:
  - bond strength remains the same as spontaneous bond
- 300°C - 800°C:
  - voids can be formed (possibly due to water molecules)
- 800°C:
  - bond strength increases to about the fracture strength of single crystal silicon of 10 to 20 MPa (at 1000°C)
- Low temperature bonding processes have been reported
- < 150°C for 10 to 400 hrs
- Energetic particle bombardment (argon at 1.5 keV)

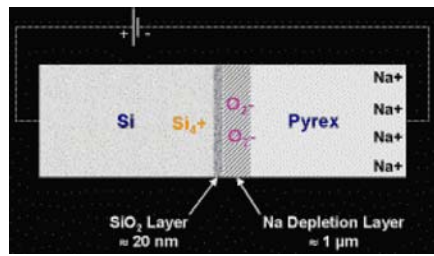
Anodic Bonding

- Joining glass to silicon
- Field-assisted thermal bonding
  - 180°C < process temperature < 500°C
  - 200 V < operating voltage < 1000 V
    - Depending on thickness and temperature
  - 5 min < process time < 10 min

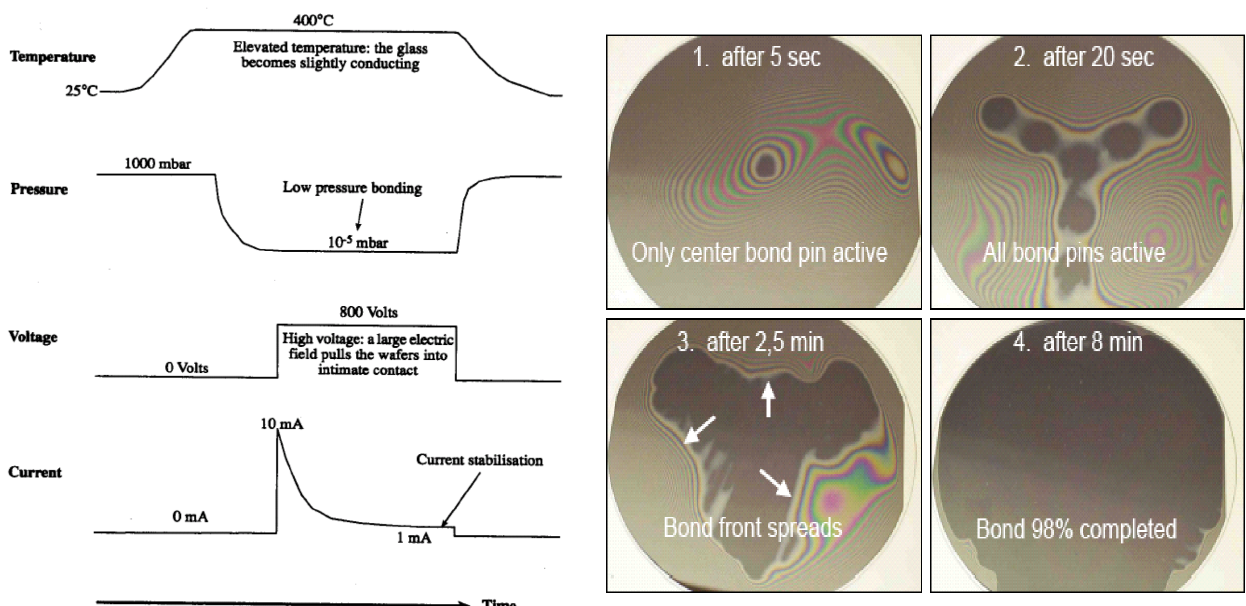


Bonding Mechanism

- Electrostatic attraction to facilitate bonding
  - Extremely mobile positive ions, mainly sodium, in the glass drift towards the negative electrode leaving a negative charge on the glass side of the silicon-glass interface
  - A high electric field is generated between this fixed negative charge and positive charge in the silicon, thus pulling the glass and silicon together and facilitating the chemical bond
  - Covalent bonds are formed



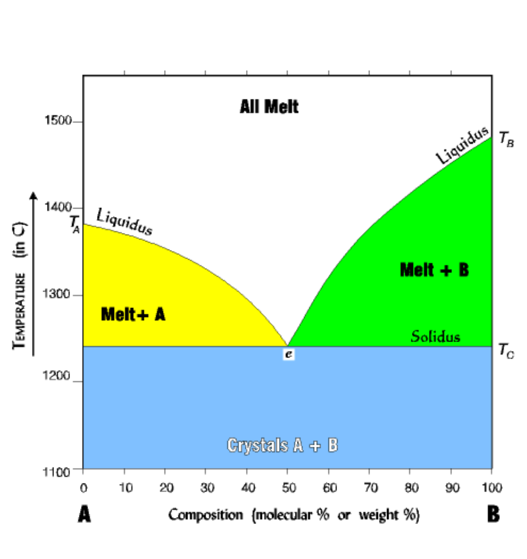
Bonding Process

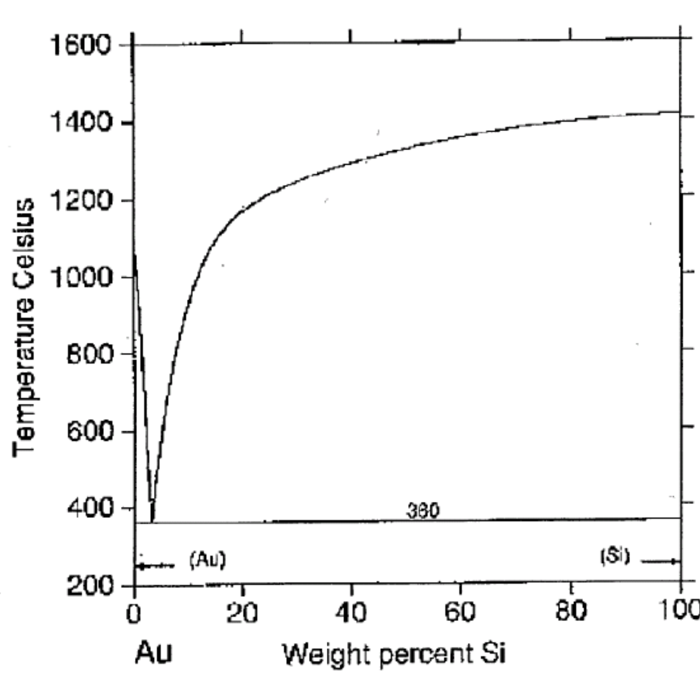


Eutectic Bonding

- Utilizing the eutectic properties of two materials combined, the combination having a lower melting point than each of the individual ones
- A typical composition is 97.1% Au and 2.85% Si by weight, which can be bonded at 386°C
- Placing the gold in contact with the silicon and heating, causing the gold atoms to diffuse into the silicon
- When the eutectic composition is reached, a liquid layer is formed at the interface and the eutectic alloy grows until the gold is exhausted
- The alloy can then be cooled slowly, causing it to solidify and hence forming the bond

Phase Diagram





Eutectic Bonding

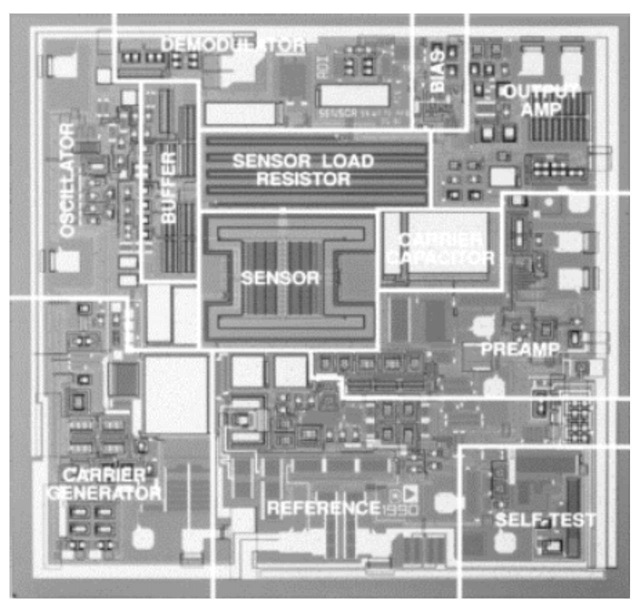
- The gold can be deposited on one of the silicon surfaces by evaporation or sputtering and functions as the intermediate layer for bonding
- The joints formed are hermetic with strength up to 148 MPa
- A drawback with this process is that the mismatch in thermal expansion coefficients results in high residual stresses within the alloy
- In addition, these stresses change with time due to creep

Adhesive Bonding

- Commercially available adhesives
- Photo-patternable polymers
- Generally can be achieved at temperatures under 150°C and are relatively soft, providing some degree of stress relief for the wafers
- They are, unsuitable for hermetic seals, can degrade over long periods of time, and can possess poor thermal stability

MEMS Packaging Issues

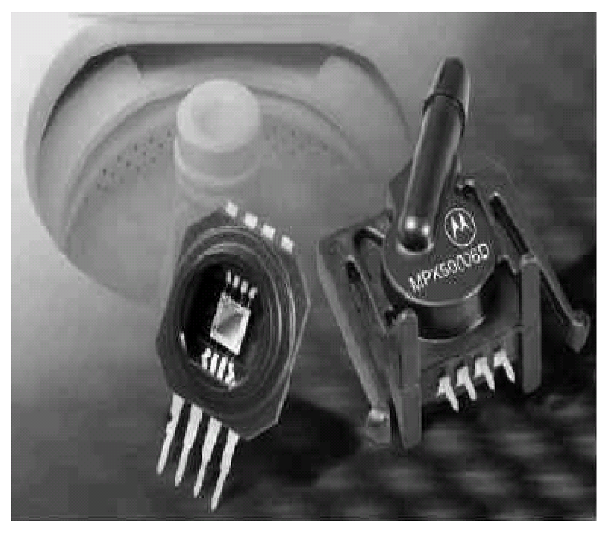
- Accelerometer
  - Surface-micromachined accelerometers by Analog Devices, Inc.
  - Free standing microstructures
  - Hermetic sealing
  - Temperature sensitive microelectronics



ADXL50 by Analog Devices, Inc.

MEMS Packaging Issues

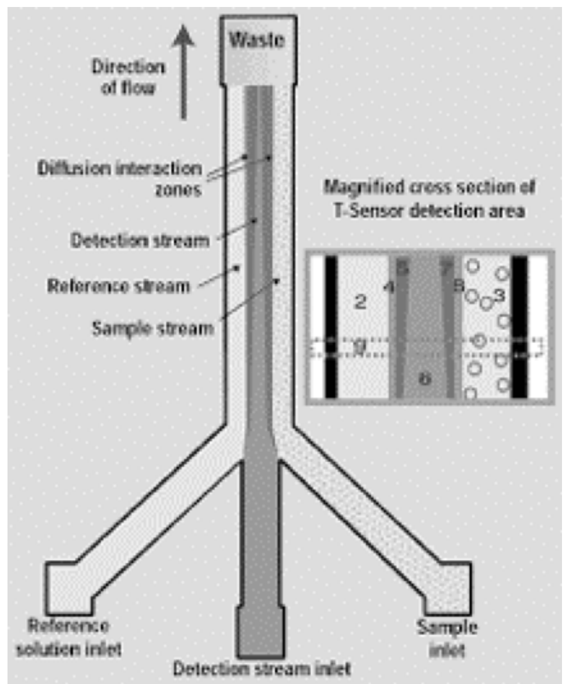
- Pressure sensor
  - Bulk micromachined pressure sensor by Motorola Inc.
  - Exposure to external pressure source
  - Housing for harsh environment
  - Interface coating



Motorola's MEMS-based pressure sensor

MEMS Packaging Issues

- Microfluidics
  - Diffusion-based sensor by Micronics
  - Micro-to-macro inter-connector
  - Good sealing
  - Temperature sensitive materials

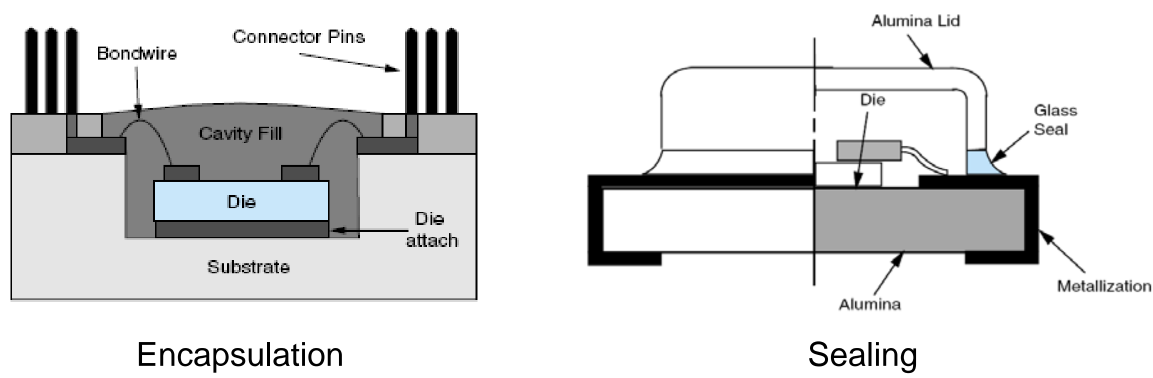


Encapsulation and Sealing

- Encapsulation provides an economical way to protect device packages by isolating the active devices from environmental pollutants, and at the same time offering mechanical protection by structural coupling of the device to the constituent packaging materials into a robust package
- This type of organic coating is a very inexpensive way of protecting devices, but their protection is not permanent, typically controlled by permeation properties of the polymeric resins used
- The inorganic sealing, however, is permanent, by being hermetic, but the cost of this process is high

Encapsulation and Sealing

- Performance is determined by its dimensional stability, its resistance to thermal excursions, its permeation providing isolation of environmental pollutants and its thermal dissipation providing dissipation of the heat generated by the packaged device



Encapsulation

Sealing

Hermetic Seal

- MIL-STD-883
- A seal that will indefinitely prevent the entry of moisture and other contaminants into the cavity
- In practice such seals are non existent
- Smaller gas molecules will enter the cavity over time by diffusion or permeation and reach equilibrium

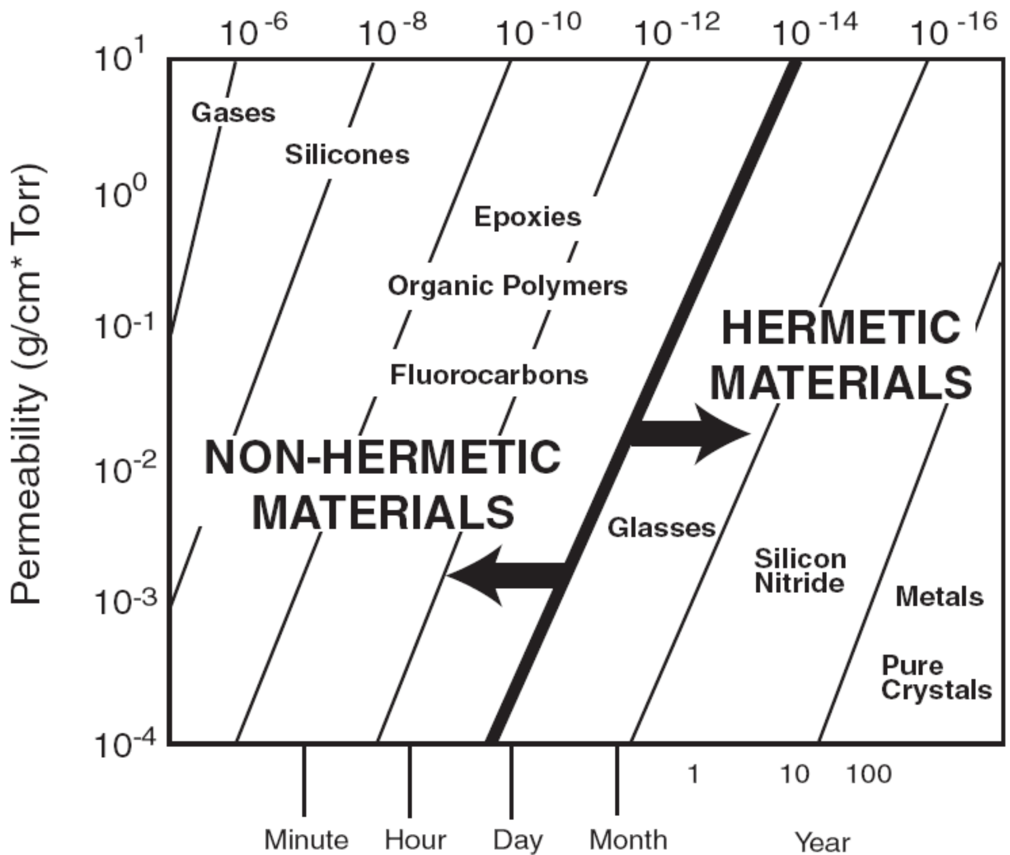


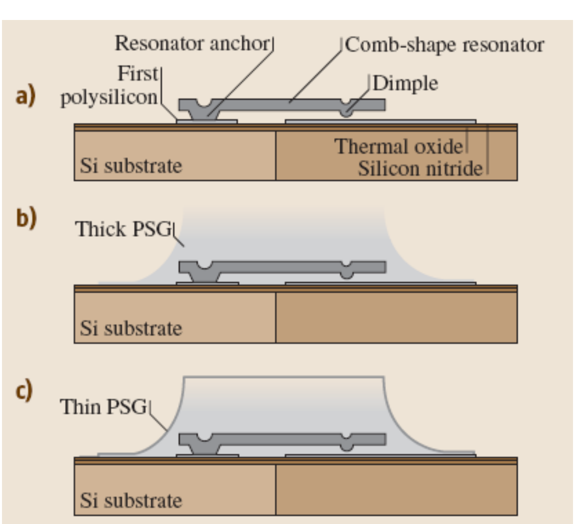
FIGURE 15.3 Permeability of water through organic (non-hermetic) and inorganic (hermetic) materials.

Hermetic Packaging

- **The permeability to moisture of glasses, ceramics and metals is orders of magnitude lower than plastic materials**
- **Metal package**
  - **harshest conditions, 80% of all metal packages are welded, with the remaining being soldered**
- **Ceramic package**
  - **Solder glass seal by high-lead-content vitreous or de-vitrifying glasses at 400°C**
  - **Hard glass seal by high-melting borosilicate glass at 1100°C**

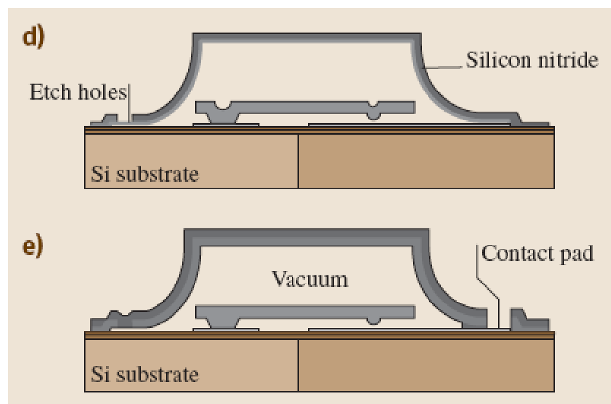
Encapsulation Processes

- LPCVD process
- (a) standard surface micromachining process
- (b) additional thick PSG deposition to define encapsulation regions
- (c) additional thin PSG deposition to define etch channels



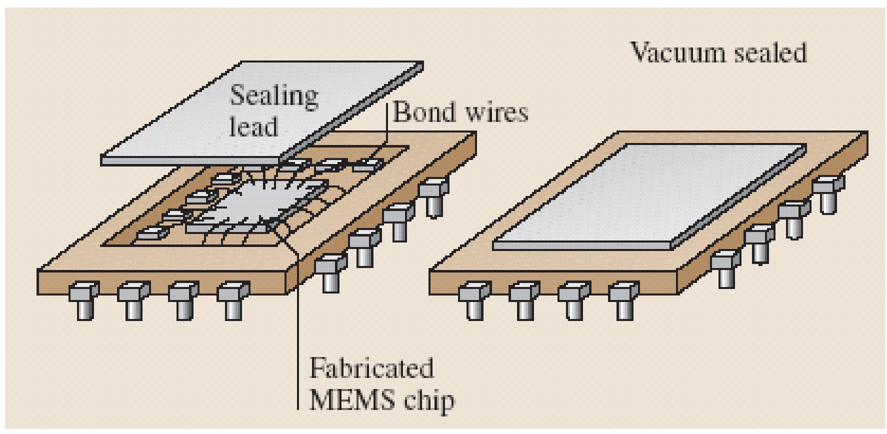
Encapsulation Processes

- LPCVD process
- (d) nitride shell deposition; etch hole definition
- (e) removal of all sacrificial PSG inside the shell; supercritical CO_2 drying; global LPCVD sealing



Packaging Process

- Electrical interconnects
- Die attachment
- Sealing



Electrical Interconnects

- Wire bonding
- Tape automated bonding
- Flip chip
  - Placing the die face-down (flipped) onto the package or circuit board
  - The electrical connection is made by conductive bumps formed on the die bond pads

Die
Bumps
Underfill
Substrate

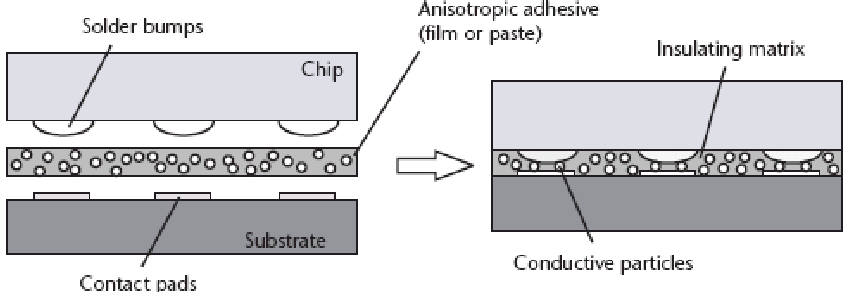
Process

Three stages

(1) Bumping the die or wafer

(2) Attaching the bumped die to the board or substrate

(3) Underfilling the remaining space under the die with an electrically insulating material



Advantages

- Reduced package size
- High-speed electrical performance due to the shortened path length
- Greater flexibility of contact pad location
- Mechanically rugged
- Lowest cost interconnection method for high-volume production

Die attachment

- Adhesive die attach
- Soldering die attach
- Eutectic bonding
- Glass die attach

Table 4.2 Relative Merits of Die Attachment Methods

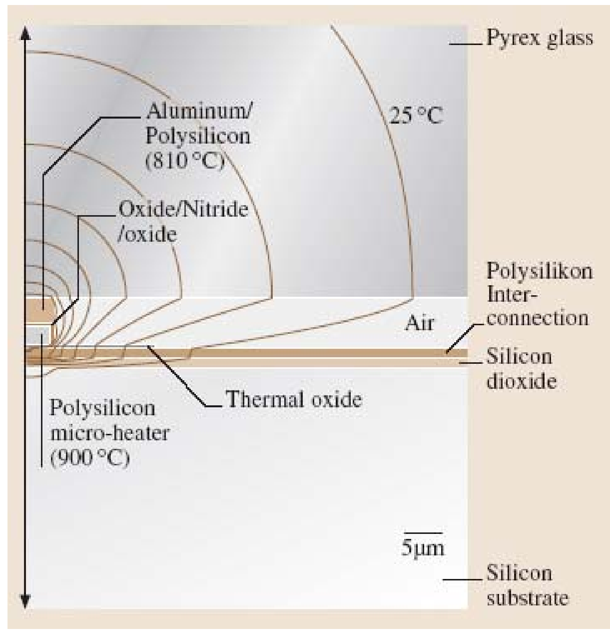
Process	*Advantages*	*Disadvantages*
Adhesive	Low cost	Outgases
	Easily automated	Contamination/bleed
	Low curing temperatures	Susceptible to voids
	Reduced die stress	Inferior thermal/electrical conductivity
	Special plated surfaces not required	Can require careful storage (e.g., –40°C) and mixing before use
	Rework possible	Not suited to harsh environments
Solder	Good electrical/thermal conductivity	Requires wettable metallized surfaces on the die and substrate
	Good absorption of stresses arising from of thermal expansion coefficients mismatches	Usually requires processing temperatures greater than 200°C
	"Clean"	Needs flux or an inert gas atmosphere
	Rework possible	Porosous
		Poor thermal fatigue resistance of some alloys
Eutectic	Good thermal conductivity	Poor absorption of stresses arising from of thermal expansion coefficients mismatches
	Electrically conducting	High processing temperatures
	Good fatigue/creep resistance	Die back metallization may be required
	Low contamination	If bare die are used, a scrubbing action is required to break down surface oxide
	"High" process/operating temperature capability	Rework difficult
Glass	Low void content	High processing temperature
	Good thermal/electrical conductivity	Glass requires an oxygen atmosphere, which can lead to oxidation of other plated systems
	Limited stress relaxation	Not commonly used
	Low contamination	
	High process/operating temperature resistance	

Packaging of Mechanical Sensors

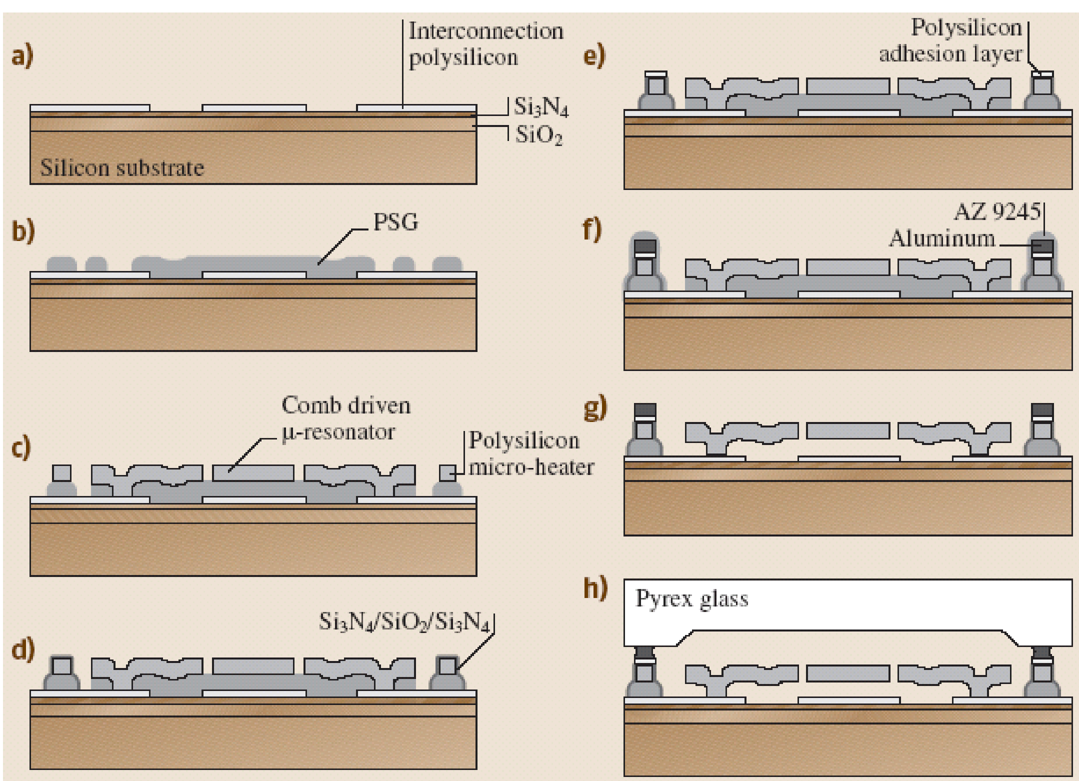
- Protect the sensor from external influences and environmental effects
- Protect the environment from the presence of the sensor
- Provide a controlled electrical, thermal, mechanical, and/or optical interface between the sensor, its associated components, and its environment

Localized Bonding

- Achieve high temperature for bonding while maintaining low temperature globally at the wafer level
- The heating region can be confined locally as long as the bottom Si substrate is constrained to the ambient temperature

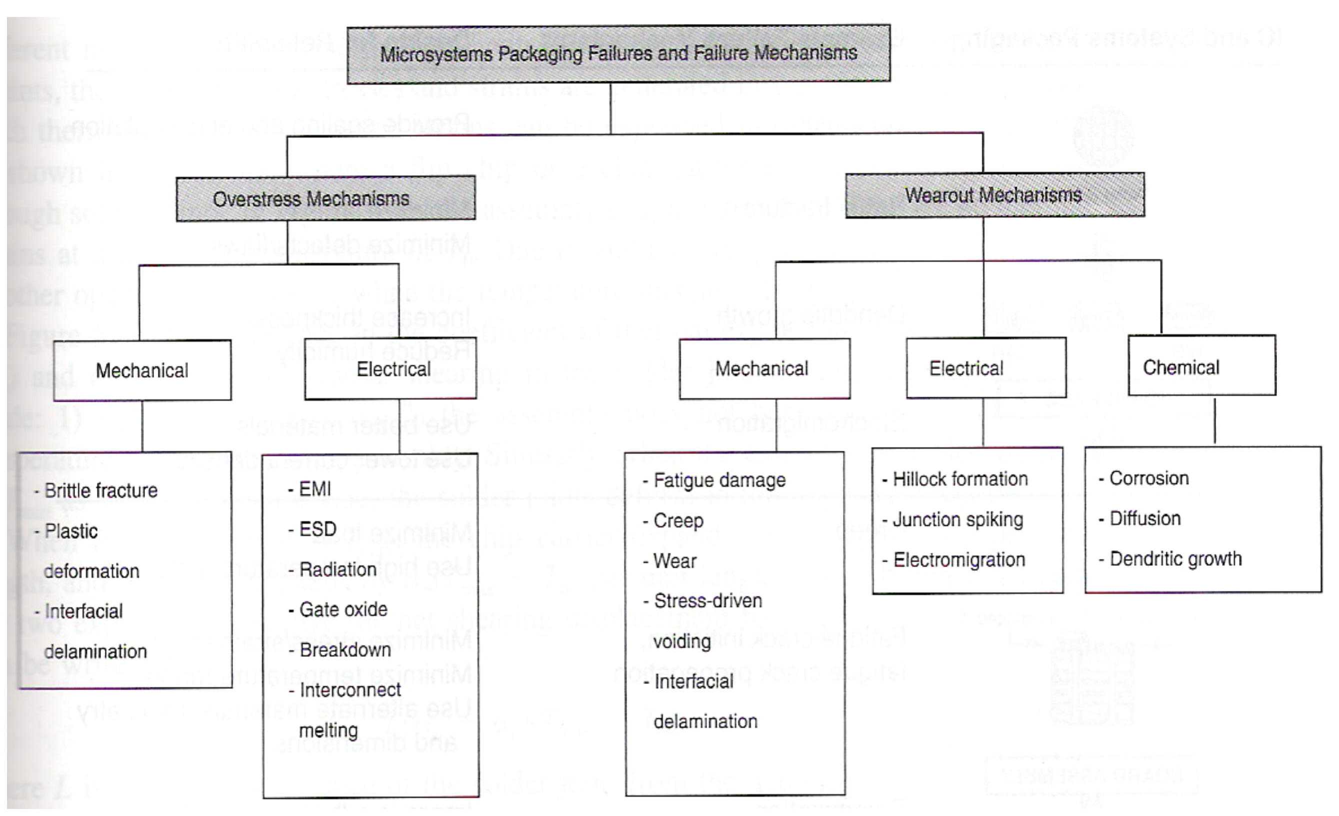


Bonding Process

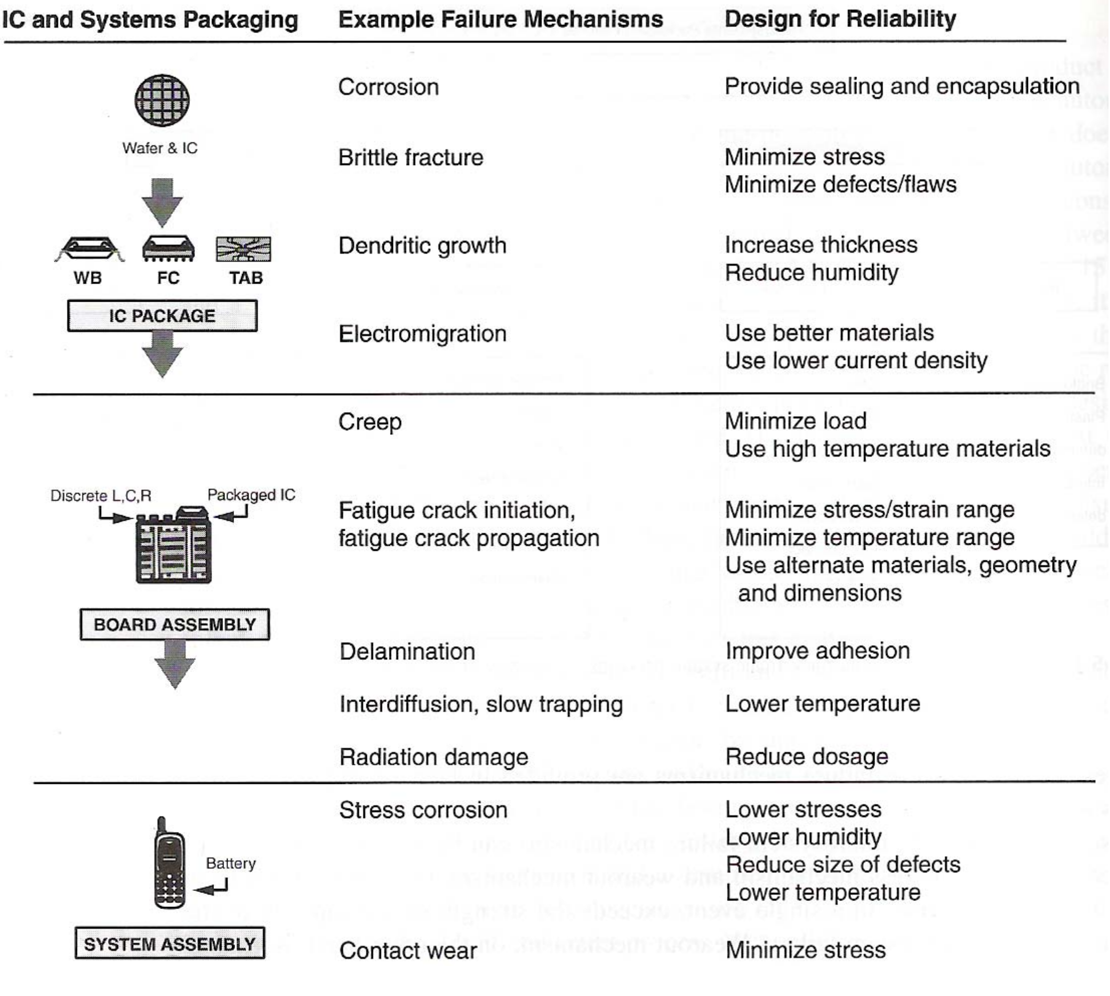


Packaging Reliability

- Testing is required before a new device can be delivered to the market
- Provide the information for the following improvement of packaging design and fabrication
- Use mathematical tools to evaluate data to understand the patterns and identify the sources of failure



Microsystems Packaging Failures and Failure Mechanisms
Overstress Mechanisms
Wearout Mechanisms
Mechanical
Electrical
Mechanical
Electrical
Chemical
- Brittle fracture
- Plastic deformation
- Interfacial delamination
- EMI
- ESD
- Radiation
- Gate oxide
- Breakdown
- Interconnect melting
- Fatigue damage
- Creep
- Wear
- Stress-driven voiding
- Interfacial delamination
- Hillock formation
- Junction spiking
- Electromigration
- Corrosion
- Diffusion
- Dendritic growth



IC and Systems Packaging
Example Failure Mechanisms
Design for Reliability
Wafer & IC
WB
FC
TAB
IC PACKAGE
Corrosion
Provide sealing and encapsulation
Brittle fracture
Minimize stress
Minimize defects/flaws
Dendritic growth
Increase thickness
Reduce humidity
Electromigration
Use better materials
Use lower current density
Discrete L,C,R
Packaged IC
BOARD ASSEMBLY
Creep
Minimize load
Use high temperature materials
Fatigue crack initiation, fatigue crack propagation
Minimize stress/strain range
Minimize temperature range
Use alternate materials, geometry and dimensions
Delamination
Improve adhesion
Interdiffusion, slow trapping
Lower temperature
Radiation damage
Reduce dosage
Battery
SYSTEM ASSEMBLY
Stress corrosion
Lower stresses
Lower humidity
Reduce size of defects
Lower temperature
Contact wear
Minimize stress

Accelerated Tests

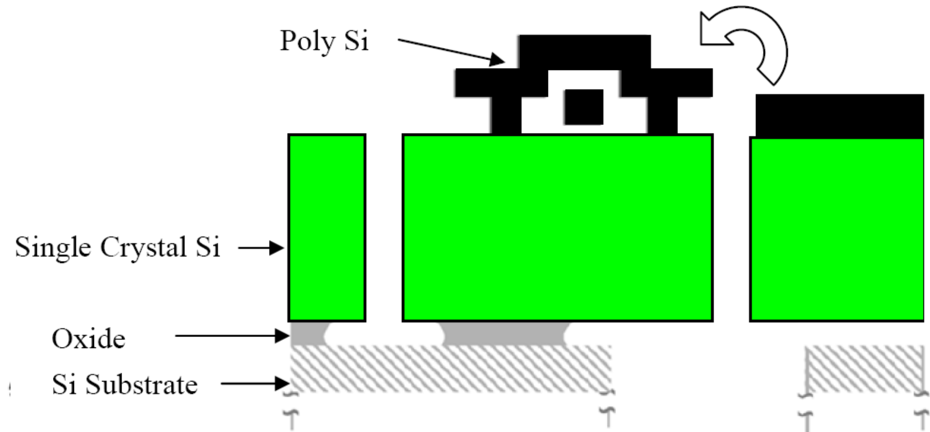
- Puts a large amount of samples in harsh environments, such as elevated temperature, elevated pressure, and 100% humidity, to accelerate the corrosion process
- The statistical failure data are gathered and analyzed to predict the lifetime of packages under normal usage environment
- As a result, the long-term reliability of the package can be predicted without going through the true long-term tests

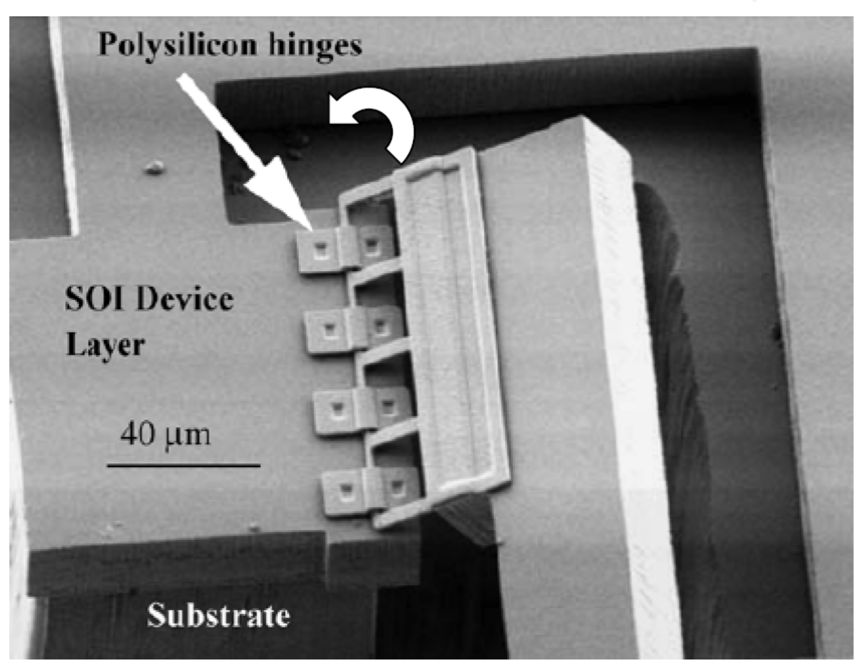
Future Trends

- Development of mechanical, thermal, and electrical models for packaging designs and fabrication processes
- Wafer-level, chip-scale packaging with low packaging cost and high yield
- Effective testing techniques at the wafer level to reduce the testing costs
- Device integrations by vertical through-interconnects as an interposer to avoid thermal mismatch problems

Part II Process Integration (24%)

1. Please design a fabrication process for the following structure. (18%)





Process description	Top/bottom view	Cross-sectional view
1 2 3 4 5		SOI wafer

2. Please design a fabrication process for the following structure. (6%)

Process description	Cross-sectional view
1 2 3 4