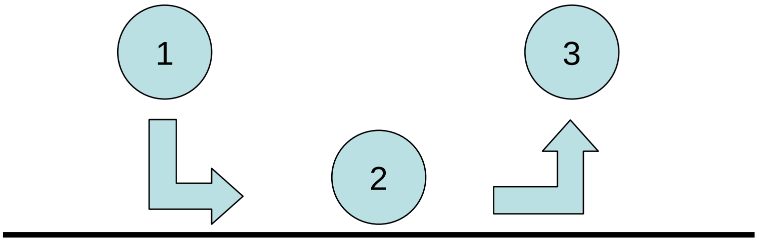
Wet Etching

ESS4810 Lecture
Fall 2010

Introduction

- Selective removal of specific materials
- Chemical process
- Isotropic etching
- Anisotropic etching
- Advantages
  - Simple, inexpensive
- Disadvantage
  - Poor process control

Wet Etching



1. Reactant transport to surface
2. Selective and controlled reaction of etchant with the film to be etched
3. Transport of by-products away from the surface

Etching of Silicon

Isotropic Etching of Silicon

- HNA system
  - HNO_3
  - HF
  - CH_3COOH or H_2O (as a diluent)

$$HNO_3 + H_2O + HNO_2 \rightarrow 2HNO_2 + 2OH^- + 2H^+$$

$$Si^{4+} + 4OH^- \rightarrow SiO_2 + H_2$$

$$6HF + SiO_2 \rightarrow H_2SiF_6 + 2H_2O$$

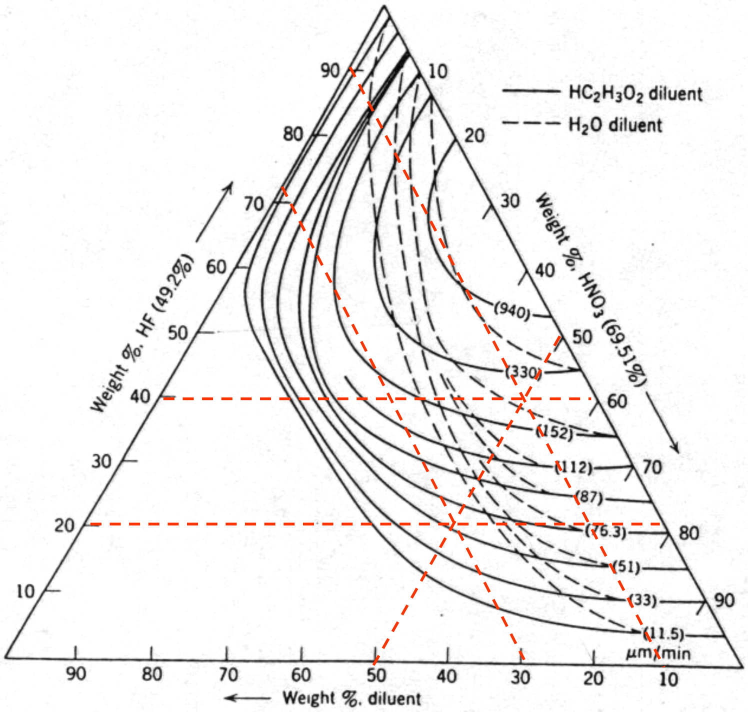
$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2$$

Etching Profiles

With agitation

Without agitation

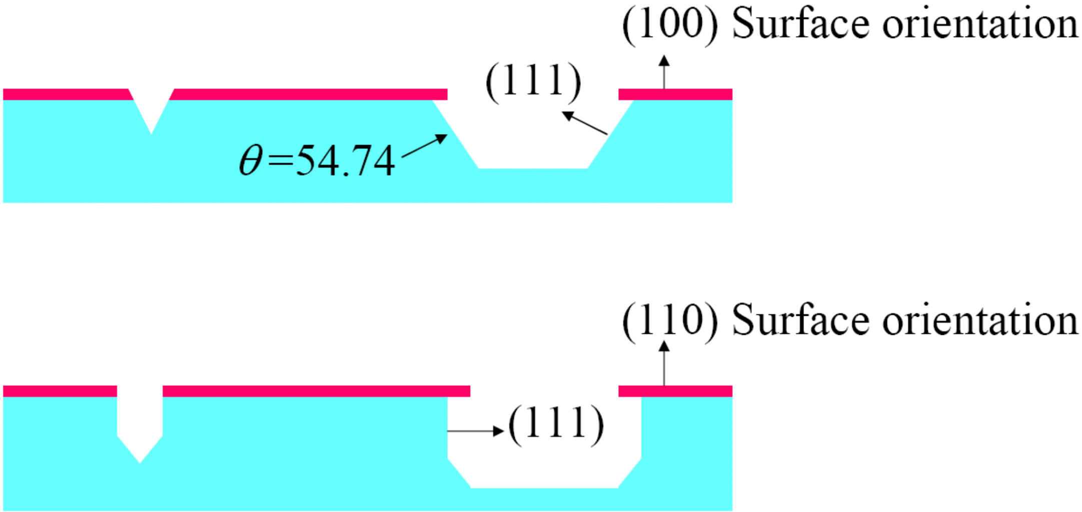
Iso-Etch Curves



Masking Materials

Mask	Piranha (4:1, H_2O_2:H_2SO_4)	Buffered HF (5:1 NH_4F:conc. HF)	HNA
Thermal SiO_2		0.1 μm/min	300–800 Å/min; limited etch time, thick layers often are used due to ease of patterning
CVD (450°C) SiO_2		0.48 μm/min	0.44 μm/min
Corning 7740 glass		0.063 μ/min	1.9 μ/min
Photoresist	Attacks most organic films	Okay for short while	Resists do not stand up to strong oxidizing agents like HNO_3 and are not used
Undoped Si, polysilicon	Forms 30 Å of SiO_2	0.23 to 0.45 Å/min	Si 0.7 to 40 μm/min at room temperature; at a dopant concentration $<10^{17}$ cm^{-3} (n or p)
Black wax			Usable at room temperature
Au/Cr	Okay	Okay	Okay
LPCVD Si_3N_4		1 Å/min	Etch rate is 10–100 Å/min; preferred masking material

Anisotropic Etching



Anisotropic Etching of Silicon

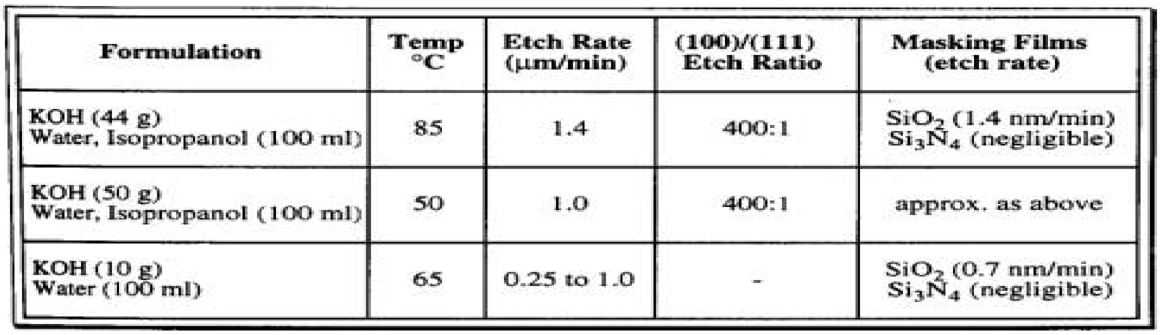
- Alkali Hydroxide (KOH, NaOH, etc.)

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2+} + 2H_2.$$

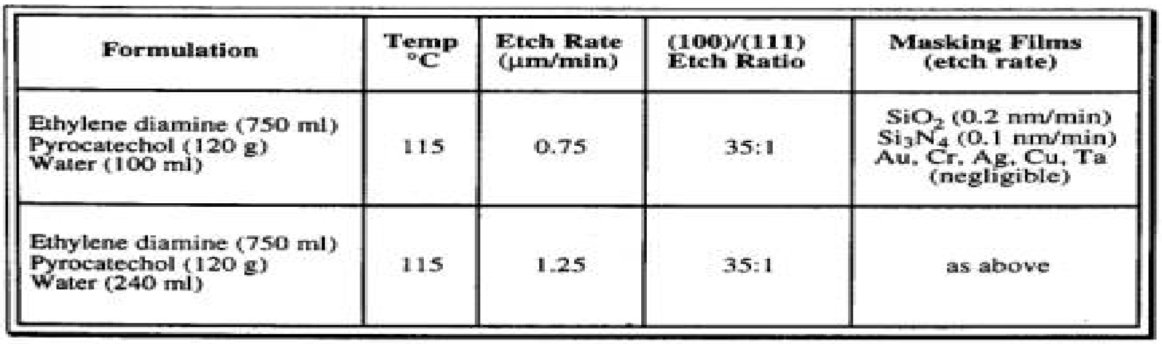
- Ethylenediamine Pyrocatechol (EDP)

$$NH_2(CH_2)_2NH_2 + H_2O \rightarrow NH_2(CH_2)_2NH_3^+ + OH^-$$
$$Si + 2OH^- + 4H_2O \rightarrow Si(OH)_6^{2-} + 2H_2$$
$$Si(OH)_6^{2-} + 3C_6H_4(OH)_2 \rightarrow [Si(C_6H_4O_2)_3]^{2-} + 6H_2O.$$

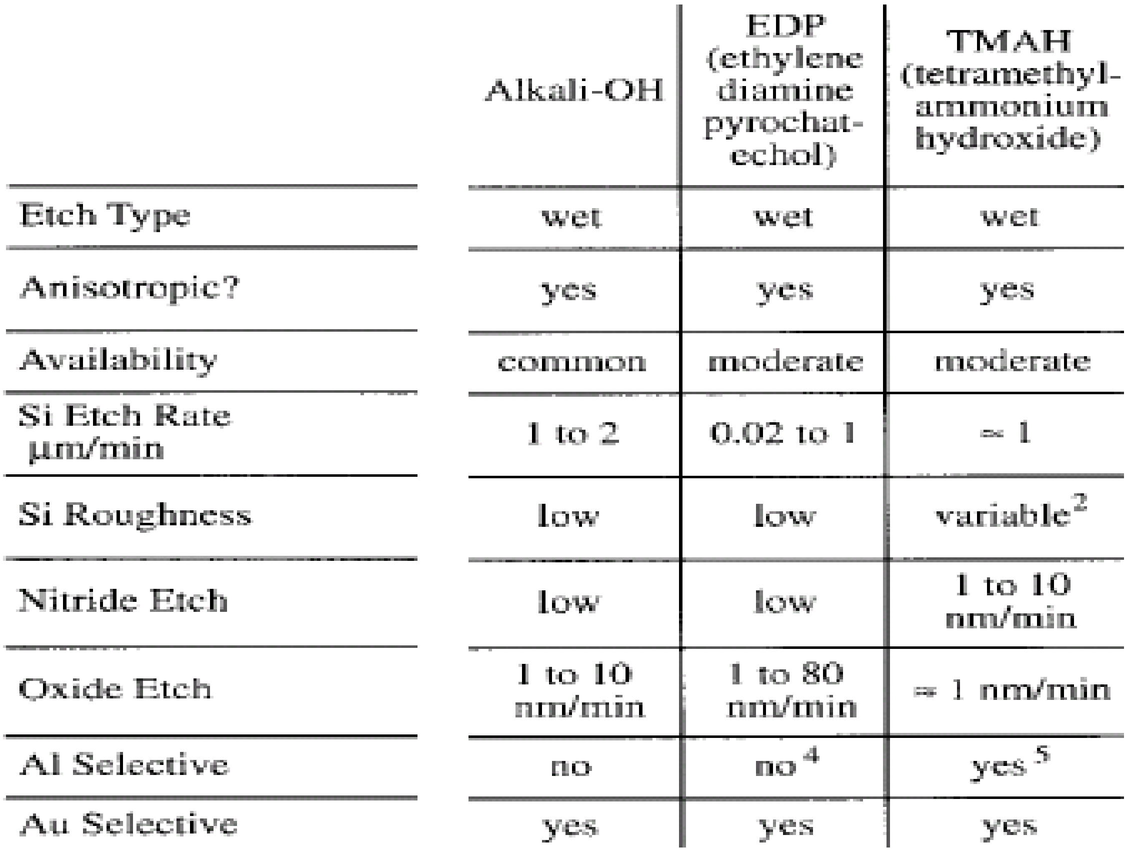
- Tetramethyl Ammonium Hydroxide (TMAH)



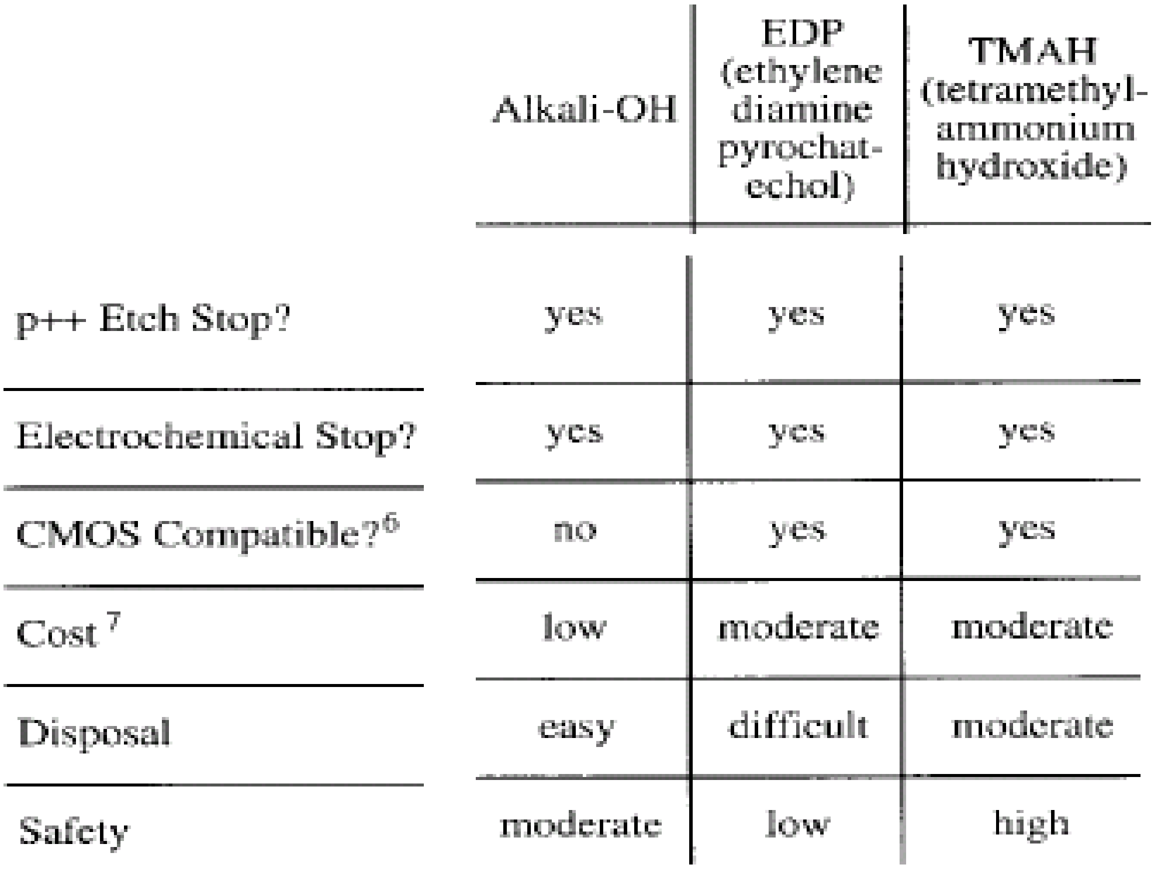
Formulation	Temp °C	Etch Rate (µm/min)	(100)/(111) Etch Ratio	Masking Films (etch rate)
KOH (44 g) Water, Isopropanol (100 ml)	85	1.4	400:1	SiO_2 (1.4 nm/min) Si_3N_4 (negligible)
KOH (50 g) Water, Isopropanol (100 ml)	50	1.0	400:1	approx. as above
KOH (10 g) Water (100 ml)	65	0.25 to 1.0	-	SiO_2 (0.7 nm/min) Si_3N_4 (negligible)



Formulation	Temp °C	Etch Rate (µm/min)	(100)/(111) Etch Ratio	Masking Films (etch rate)
Ethylene diamine (750 ml) Pyrocatechol (120 g) Water (100 ml)	115	0.75	35:1	SiO_2 (0.2 nm/min) Si_3N_4 (0.1 nm/min) Au, Cr, Ag, Cu, Ta (negligible)
Ethylene diamine (750 ml) Pyrocatechol (120 g) Water (240 ml)	115	1.25	35:1	as above

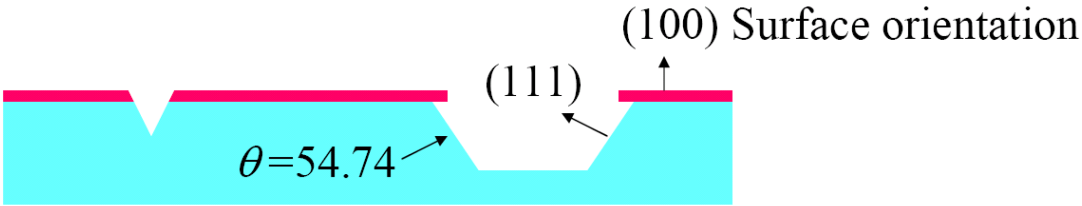


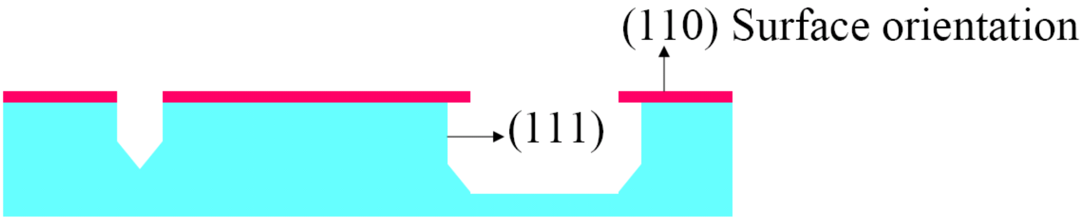
	Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide)
Etch Type	wet	wet	wet
Anisotropic?	yes	yes	yes
Availability	common	moderate	moderate
Si Etch Rate µm/min	1 to 2	0.02 to 1	≈ 1
Si Roughness	low	low	variable[2]
Nitride Etch	low	low	1 to 10 nm/min
Oxide Etch	1 to 10 nm/min	1 to 80 nm/min	≈ 1 nm/min
Al Selective	no	no [4]	yes [5]
Au Selective	yes	yes	yes



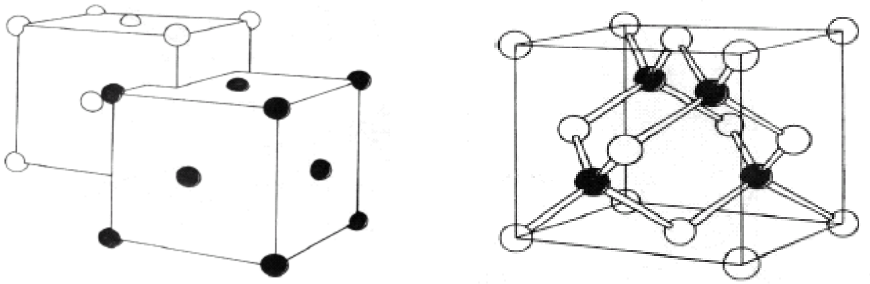
	Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide)
p++ Etch Stop?	yes	yes	yes
Electrochemical Stop?	yes	yes	yes
CMOS Compatible?[6]	no	yes	yes
Cost[7]	low	moderate	moderate
Disposal	easy	difficult	moderate
Safety	moderate	low	high

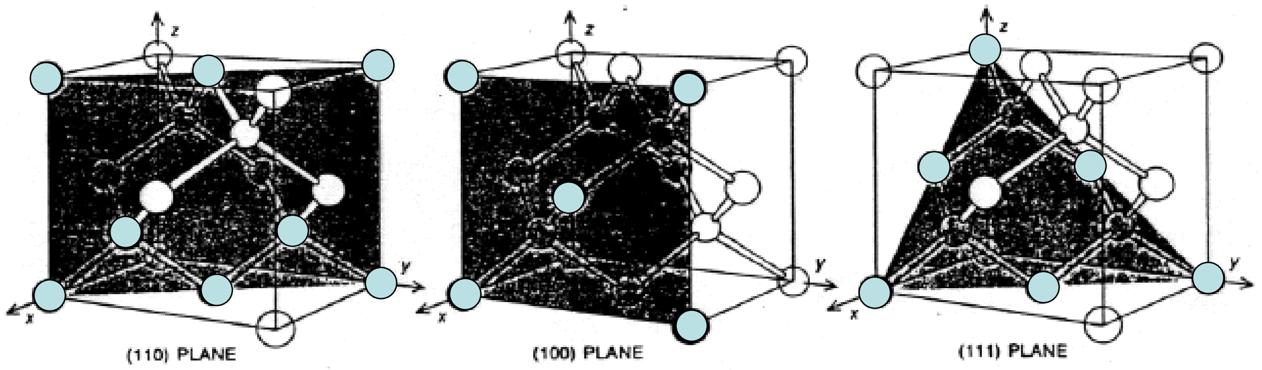
Anisotropic Etching





Silicon Crystallography





(110) PLANE (100) PLANE (111) PLANE

Miller Indices

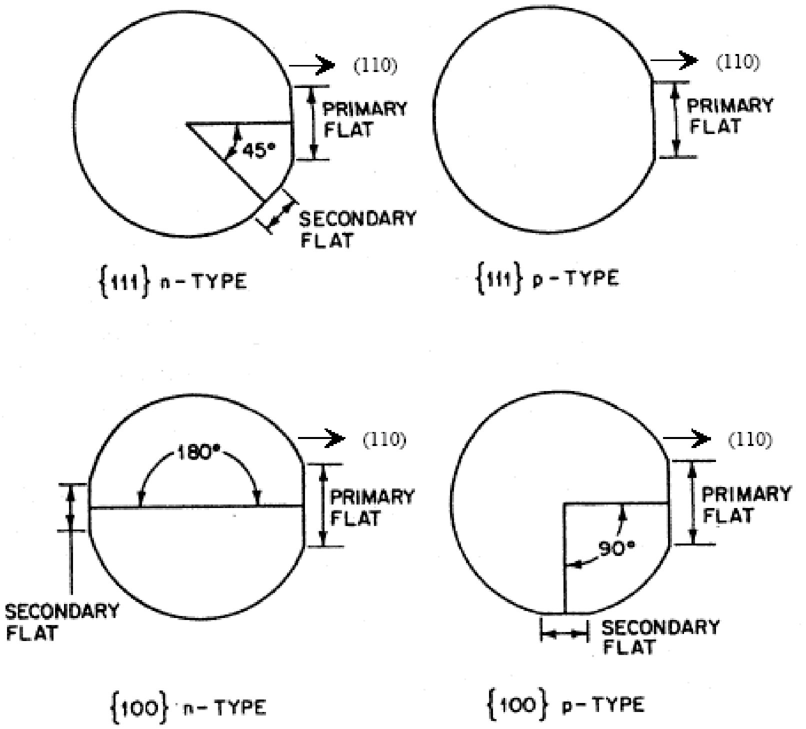
- [i, j, k]
  - a specific direction of a unit vector
- < i, j, k>
  - a family of equivalent directions
- (i, j, k)
  - a specific crystal plane
- {i, j, k}
  - a family of equivalent planes

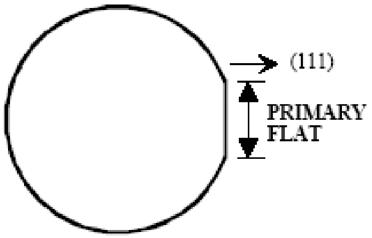
Miller Indices

- Angles between planes
  - ∠ between [abc] and [xyz] given by
  - $ax+by+cz = |(a,b,c)|*|(x,y,z)|*\cos(\Theta)$

$$\theta_{(100),(111)} = Cos^{-1}((1+0+0)/(1)(\sqrt{3}))$$

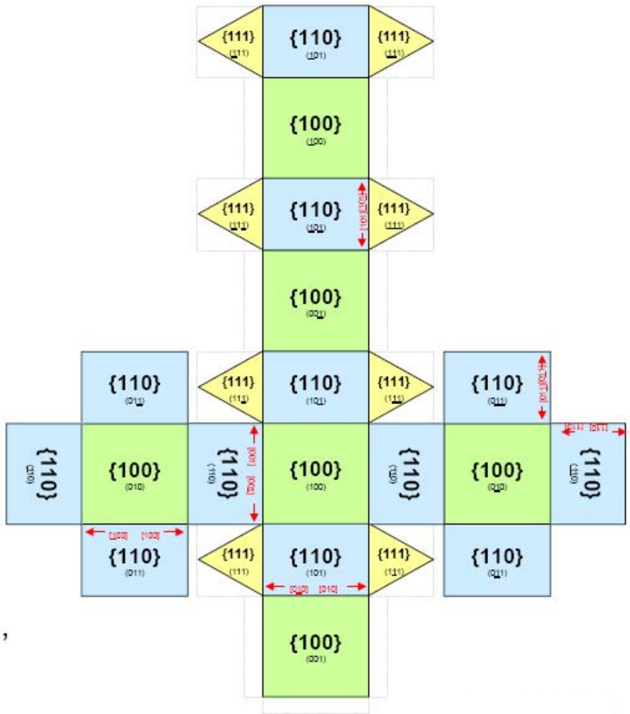
- {100} and {110}: 45°
- {100} and {111}: 54.74°
- {110} and {111}: 35.26°, 90°, and 144.74°





{110} wafer secondary flat is different from company to company

Silicon Crystallography



- Silicon fold-up cube
  - Adapted from Profs. Kris Pister and Jack Judy
  - Print onto transparency
  - Assemble inside out
  - Visualize crystal plane orientations, intersections, and directions

Lateral Underetch

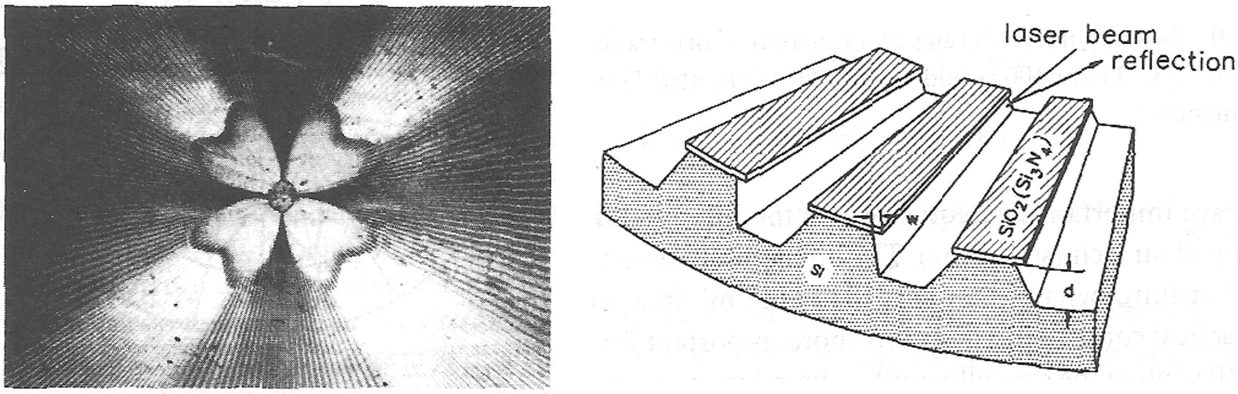
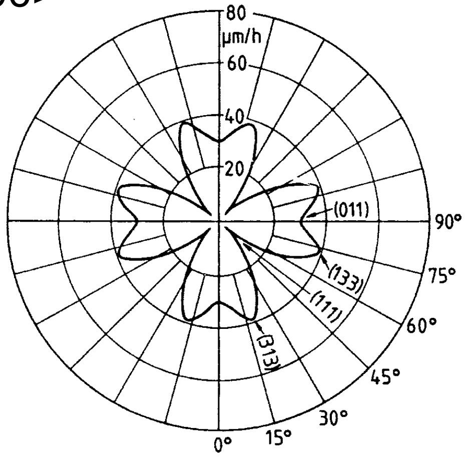
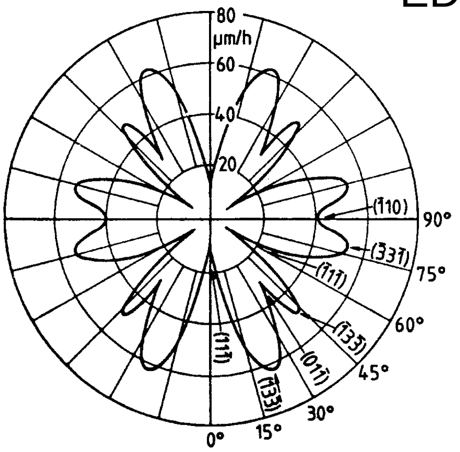


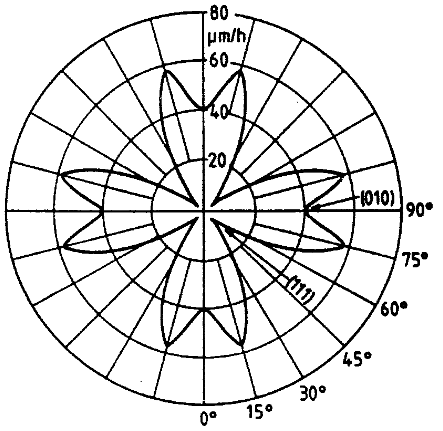
Figure 4.38 (A) Etch pattern emerging on a wagon-wheel-masked, <100>-oriented Si wafer after etching in an EDP solution. (B) Schematic cross section of a silicon test chip covered with a wagon-wheel-shaped masking pattern after etching. The measurement of *w* is used to construct polar diagrams of lateral underetch rates

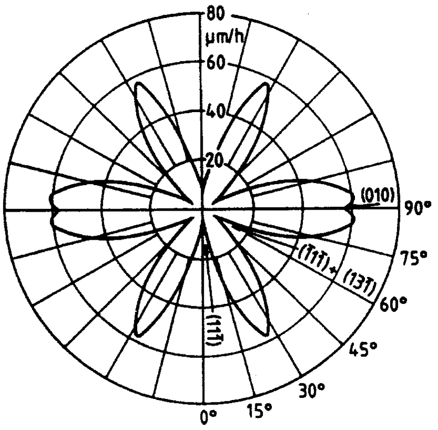
EDP <100>



EDP <110>





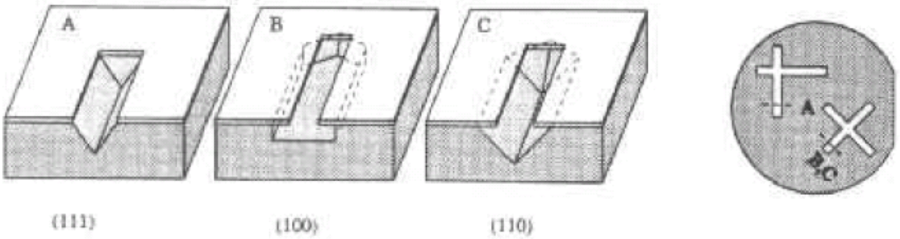


KOH <100>

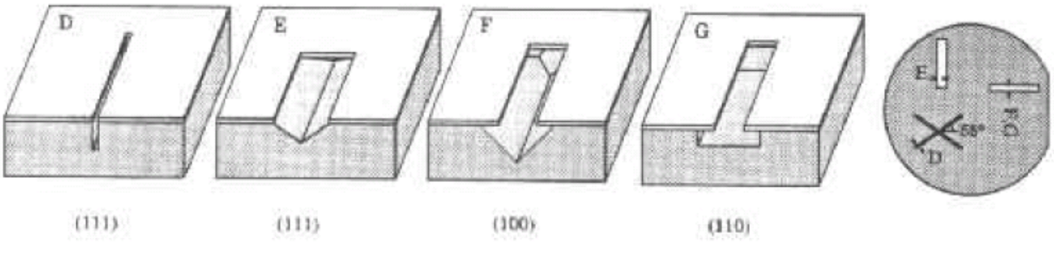
KOH <110>

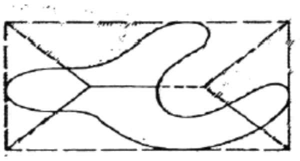
Anisotropic Etching

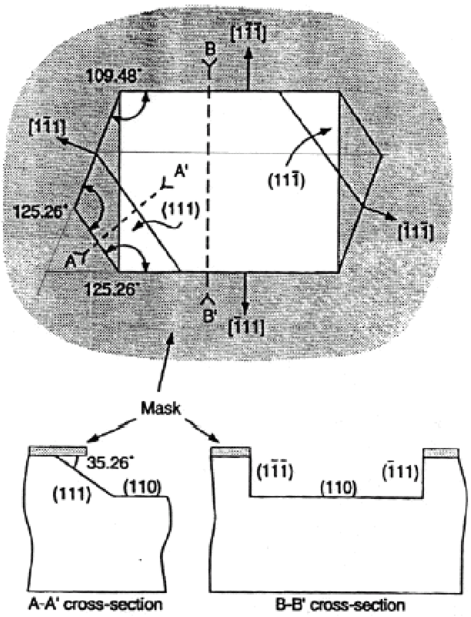
Possible v-groove cross sections on a (100) Si wafer

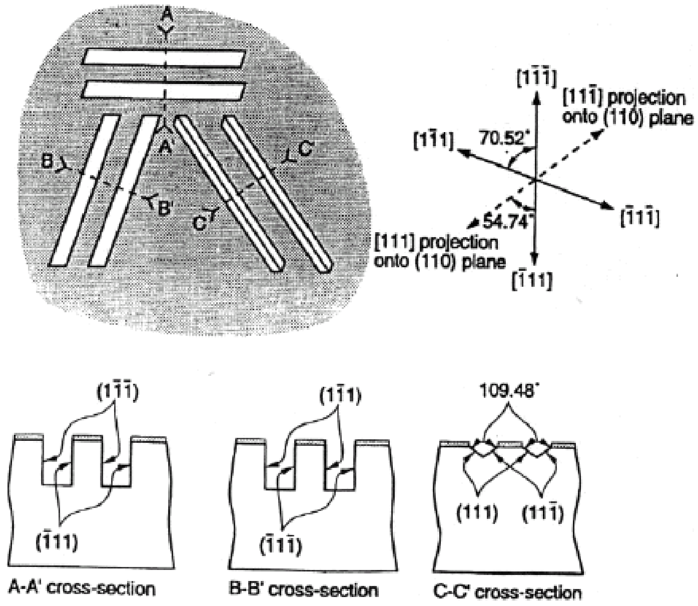


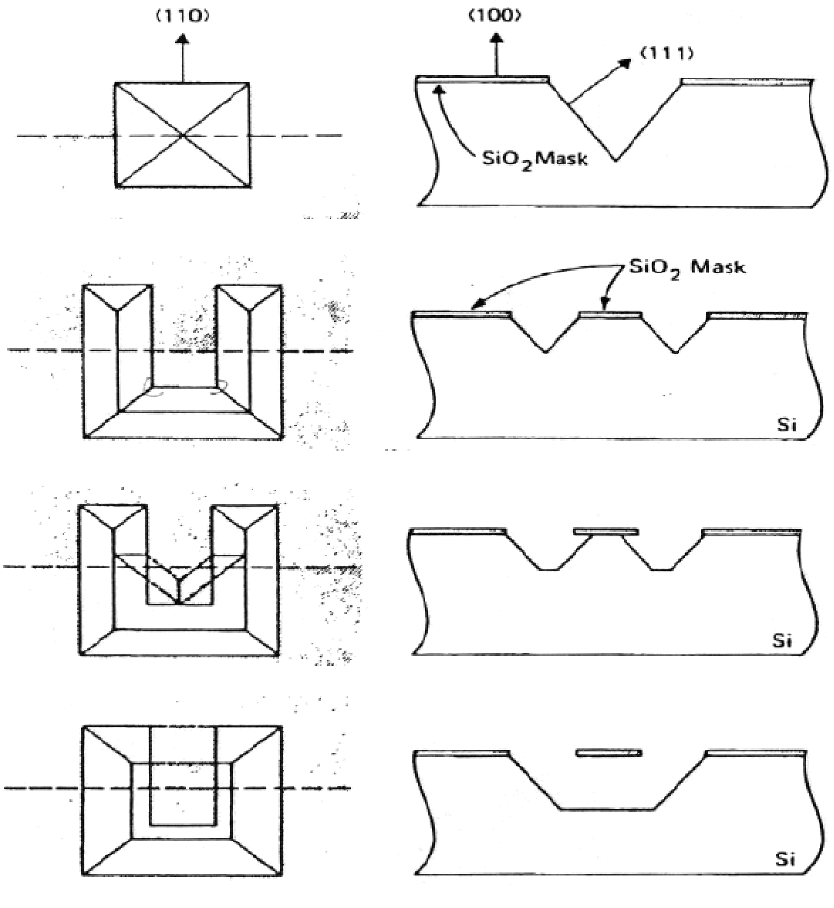
Possible v-groove cross sections on a (110) Si wafer





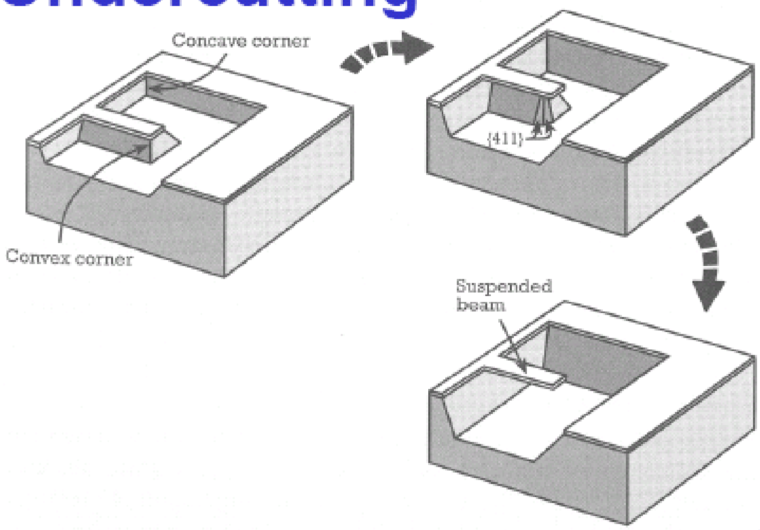

[11̄1̄]
B
109.48°
[11̄1]
A'
(111)
(111̄)
[111̄]
125.26°
A
125.26°
B'
[1̄11]
Mask
35.26°
(111)
(110)
(11̄1̄)
(110)
(1̄11)
A-A' cross-section
B-B' cross-section


A
A'
B
B'
C
C'
[11̄1̄]
[111̄] projection onto (1̄10) plane
[11̄1]
70.52°
[1̄11̄]
54.74°
[111] projection onto (110) plane
[1̄11]
(11̄1̄)
(1̄11)
A-A' cross-section
(11̄1)
(1̄11̄)
B-B' cross-section
109.48°
(111)
(111̄)
C-C' cross-section

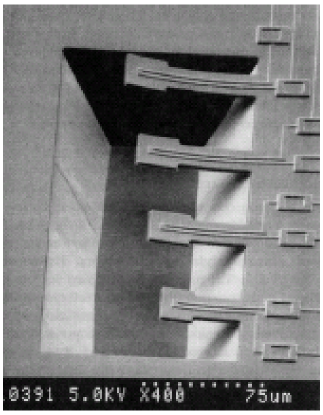

(110)
(100)
(111)
SiO₂ Mask
SiO₂ Mask
Si
Si
Si

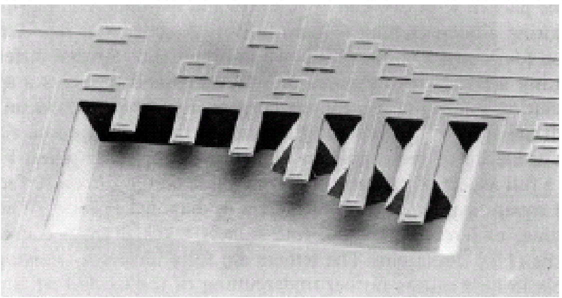
Undercutting

- Convex corners bounded by {111} planes are attacked



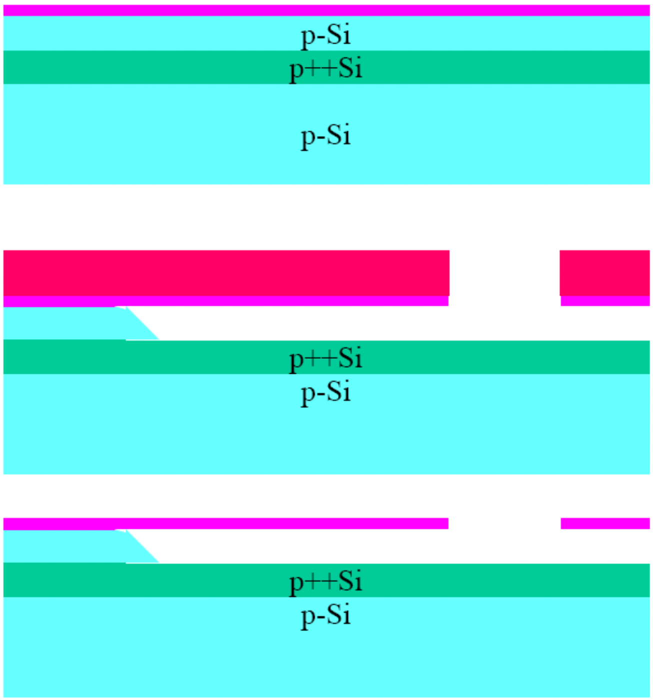
Maluf





Ristic

EDP Etching



EDP etching solution stop at the buried p++ Si layer:

Etylene diamine (750 ml)

pyrochatechol(120g)

Water(100ml)

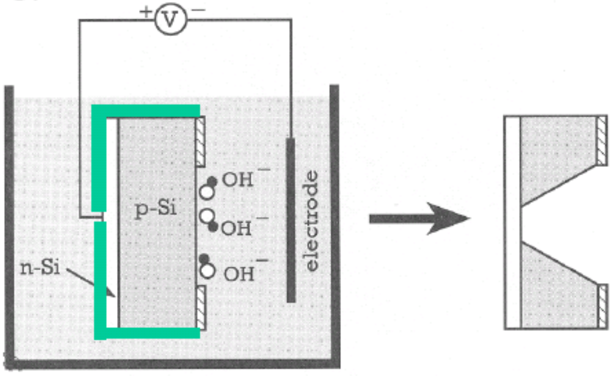
Etch rate 1.25 μm/min

@115°C

Peterson (1982)

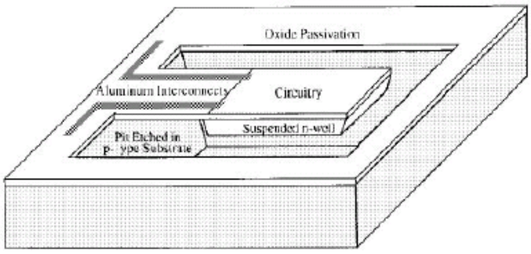
Electrochemical Etch Stop

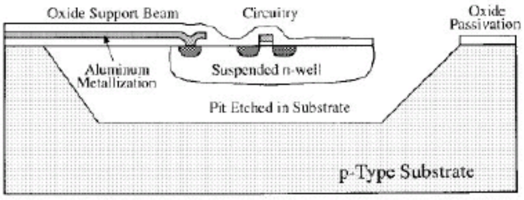
- Electrochemical etch stop
  - n-type epitaxial layer grown on p-type wafer forms p-n diode
  - p > n → electrical conduction
  - p < n → reverse bias current
  - Passivation potential – potential at which thin SiO_2 layer forms, different for p- and n-Si
- Set-up
  - p-n diode in reverse bias
  - p-substrate floating → etched
  - n-layer above passivation potential → not etched

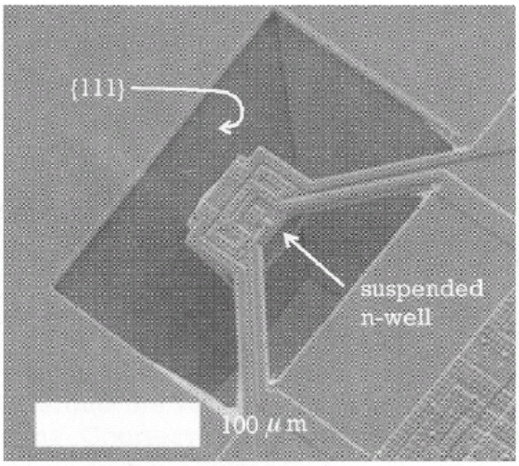


Electrochemical Etch Stop

- Electrochemical etching on preprocessed CMOS wafers
  - N-type Si well with circuits suspended from SiO_2 support beam
  - Thermally and electrically isolated
  - TMAH etchant, Al bond pads safe







Reay et al. (1994)
Kovacs group, Stanford U.

Wet Etching of Thin Films

- Silicon dioxide
  - HF
  - Buffered HF (BHF)-10:1 HF/NH_3F "BOE"
- Silicon Nitride
  - Phosphoric acid
  - Selectivity [Si_3N_4/SiO_2] = 40/1
- Polysilicon
  - KOH, EDP, and TMAH

Wet Etching of Quartz

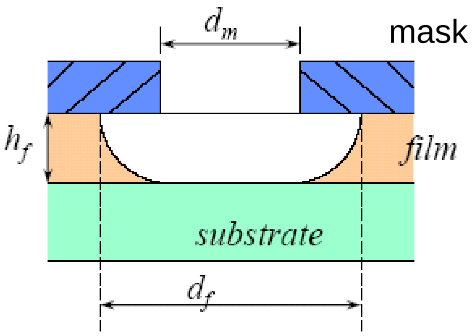
- Anisotropic etching by HF
  - with 10.9mol/l, Rate ~ 9.6 µm/hr
- Ammonium fluoride (NH_4F)
- Saturated ammonium bifluoride (NH_4HF_2)
- Require metal mask or oxide mask
- Amorphous Si or Poly Si can be used as mask for deep etching

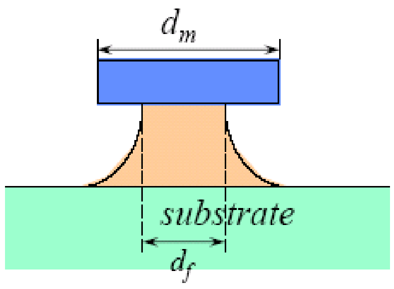
References

- K.E. Petersen, “Silicon as a Mechanical Material,” Proc. IEEE, vol. 70, pp. 420-457, May 1982
- G.T.A. Kovacs, N.I. Maluf, and K.E. Petersen, “Bulk Micromachining of Silicon,” Proc. IEEE, vol. 86, pp. 1536-1551, August 1998

Etching Bias

- Bias = d_f - d_m
- Complete isotropic etching B=$2h_f$
- Complete anisotropic etching B=0





Degree of Anisotropy

$$A_f \equiv 1 - \frac{|B|}{2h_f}$$

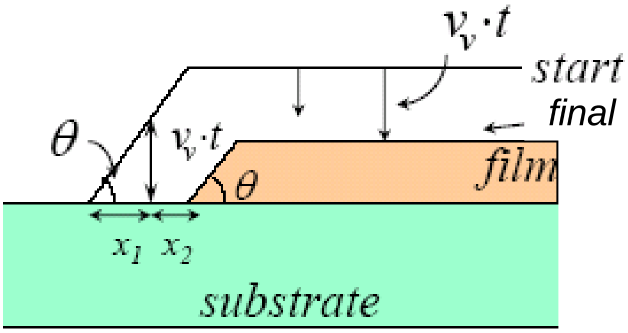
$$0 \le A_f \le 1$$

- $A_f = 0$: isotropic $\quad |B = 2h_f|$
- $A_f = 1$: anisotropic $\quad |B = 0|$

Etching of Steps with a Slope

$$x_1 = v_v \cdot t \cot\theta$$

$$x_2 = v_l \cdot t$$



Let etching time $= t$

$v_v =$ *vertical etch rate*

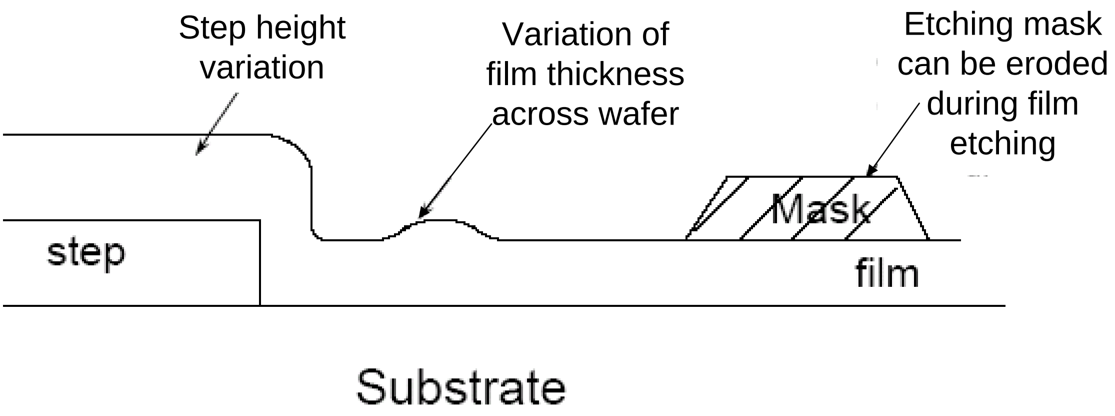
$v_l =$ *lateral etch rate*

$\therefore$ *To minimize* $x \Rightarrow$ *make* θ *large*

$$x = x_1 + x_2$$

$$= (v_v \cot\theta + v_l) \cdot t$$

Worst-Case Design Considerations for Etching



Step height variation

Variation of film thickness across wafer

Etching mask can be eroded during film etching

Design Considerations for Etching

- Film thickness variation

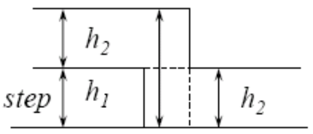
$$h_{f(\max)} = h_f \cdot (1+\delta)$$

- Film etching rate variation

$$v_{f(\min)} = v_f \cdot (1-\phi_f)$$

- Over-etching around step

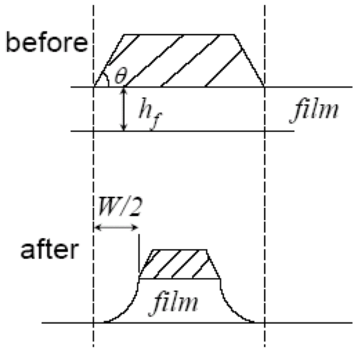
$$t_T = \frac{h_f(1+\delta)}{v_f \cdot (1-\phi_f)} \cdot (1+\frac{h_1}{h_2})$$



- With mask erosion

$$\frac{W}{2} = \left(v_{m\perp} \cot\theta + v_{m//}\right) \cdot t_T$$

$$= \left(\frac{v_{m\perp}}{v_f}\right) \cdot h_f \cdot \frac{(1+\delta)(1+\Delta)}{\left(1-\phi_f\right)} \left[\cot\theta + \frac{v_{m//}}{v_{m\perp}}\right]$$



Bulk Micromachining of Silicon

ESS4810 Lecture
Fall 2010

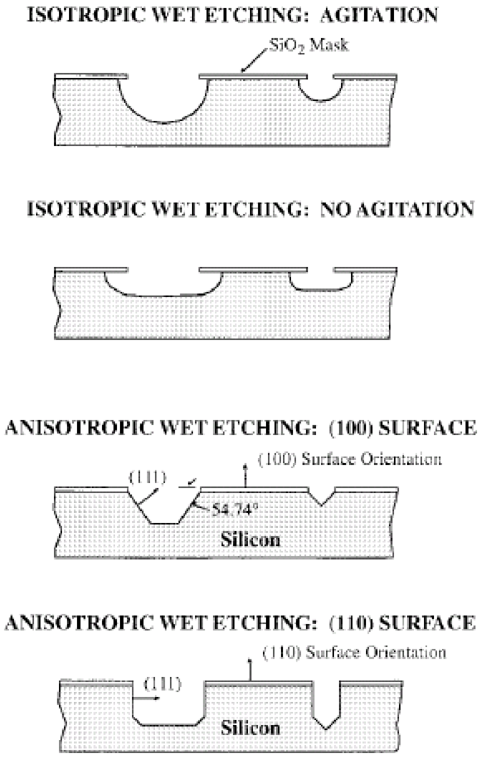
Introduction

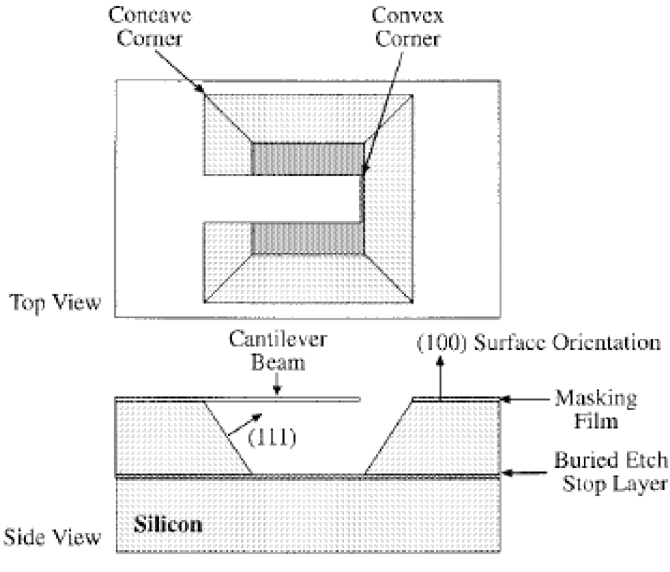
- Purpose of bulk micromachining
  - Selectively remove significant amounts of silicon from a substrate
- Three categories
  - In terms of the state of the etchant
  - Wet, vapor, and plasma
- The majority of currently shipping silicon sensors are made using bulk etching

Purposes

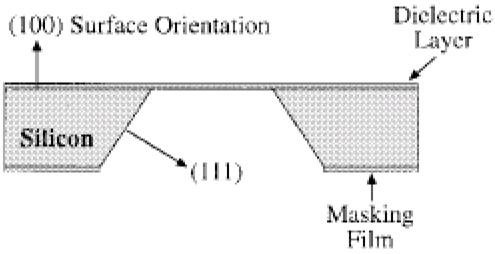
- To undercut structures that are required to physically move
- To form membranes on one side of a wafer
- To make a variety of trenches, holes, or other structures

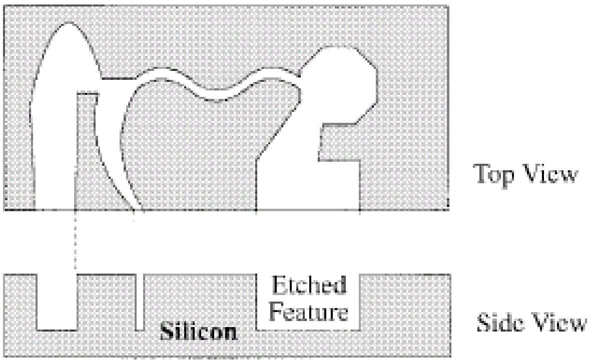
Possible Machined Structures

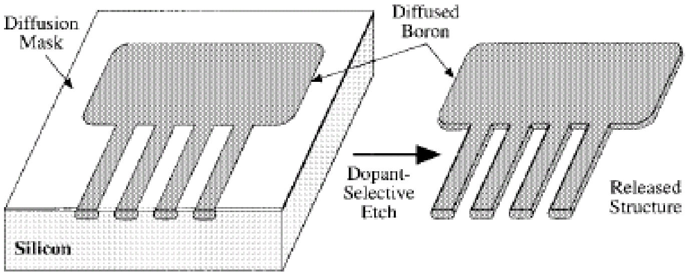




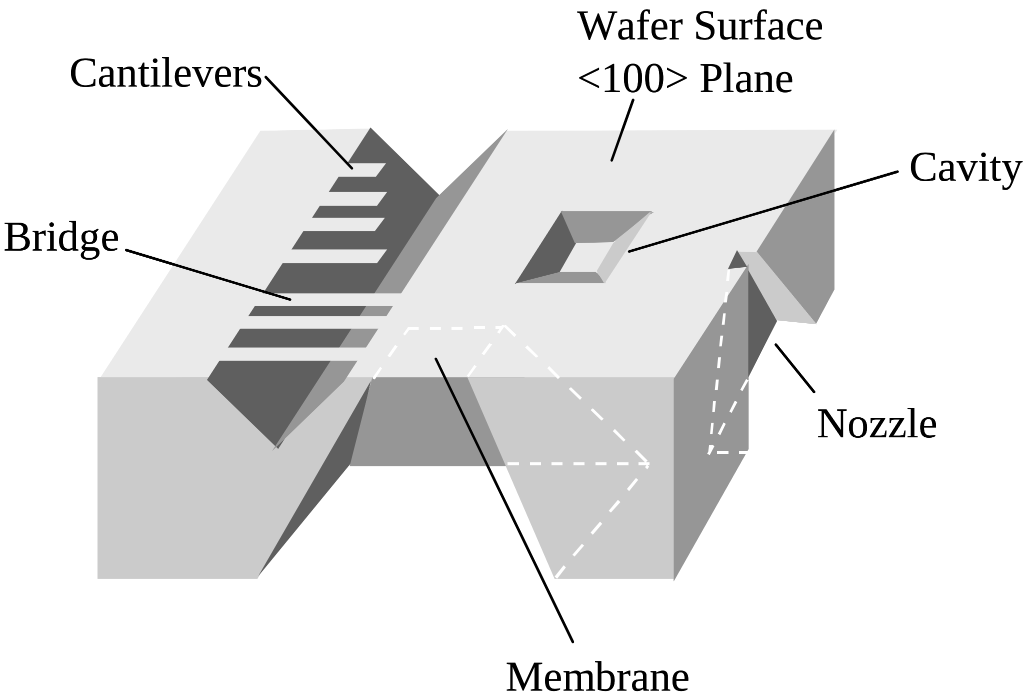
Possible Machined Structures



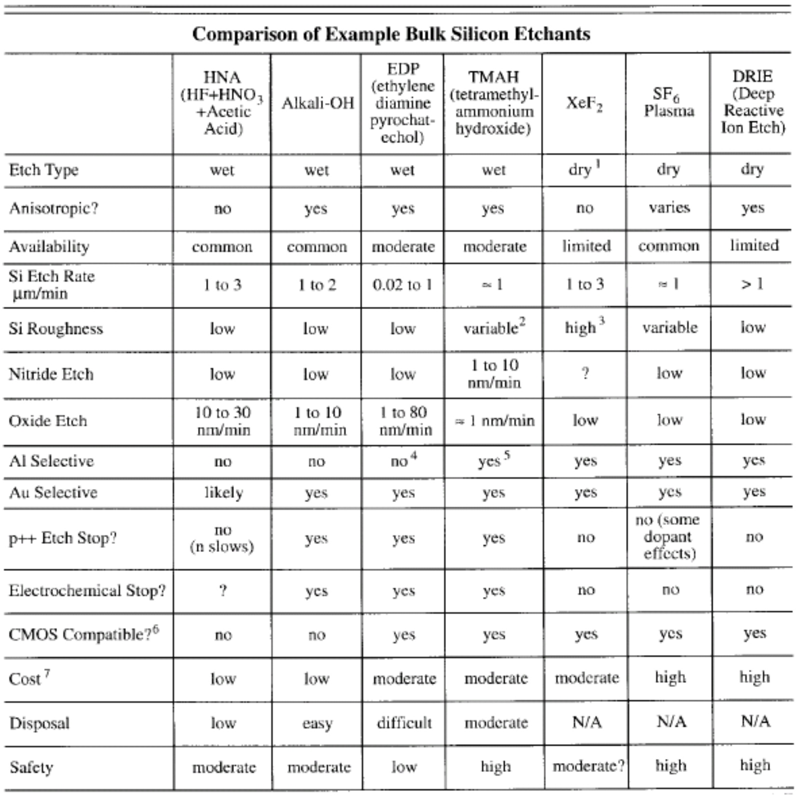




Possible Machined Structures



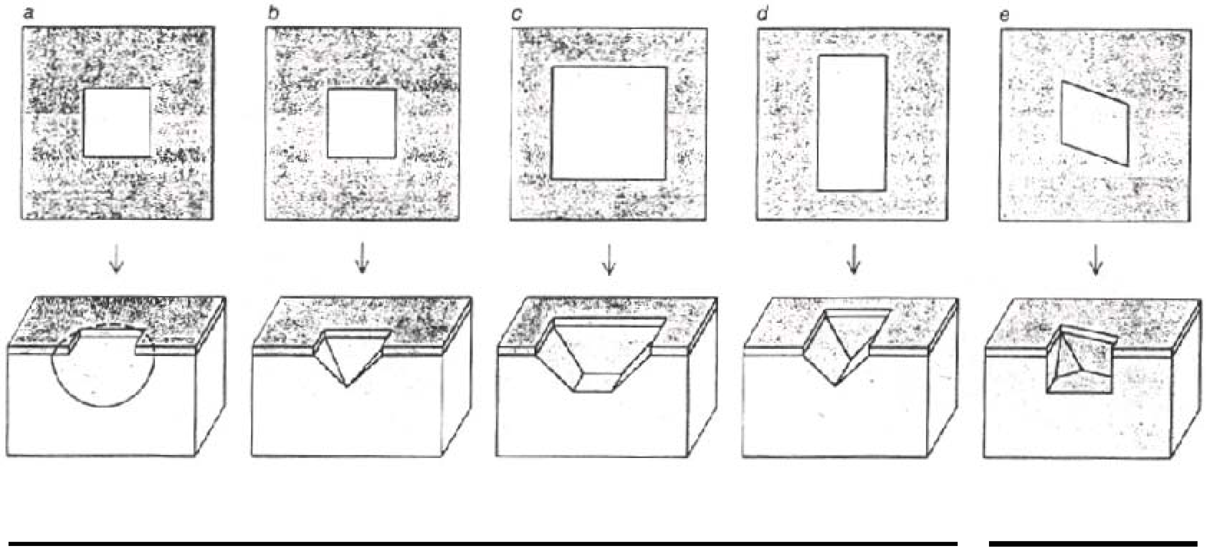
Comparison of Silicon Etchants



Comparison of Example Bulk Silicon Etchants

	HNA (HF+HNO$_3$ +Acetic Acid)	Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide)	XeF$_2$	SF$_6$ Plasma	DRIE (Deep Reactive Ion Etch)
Etch Type	wet	wet	wet	wet	dry[1]	dry	dry
Anisotropic?	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Si Etch Rate μm/min	1 to 3	1 to 2	0.02 to 1	≈ 1	1 to 3	≈ 1	> 1
Si Roughness	low	low	low	variable[2]	high[3]	variable	low
Nitride Etch	low	low	low	1 to 10 nm/min	?	low	low
Oxide Etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	≈ 1 nm/min	low	low	low
Al Selective	no	no	no[4]	yes[5]	yes	yes	yes
Au Selective	likely	yes	yes	yes	yes	yes	yes
p++ Etch Stop?	no (n slows)	yes	yes	yes	no	no (some dopant effects)	no
Electrochemical Stop?	?	yes	yes	yes	no	no	no
CMOS Compatible?[6]	no	no	yes	yes	yes	yes	yes
Cost[7]	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate?	high	high

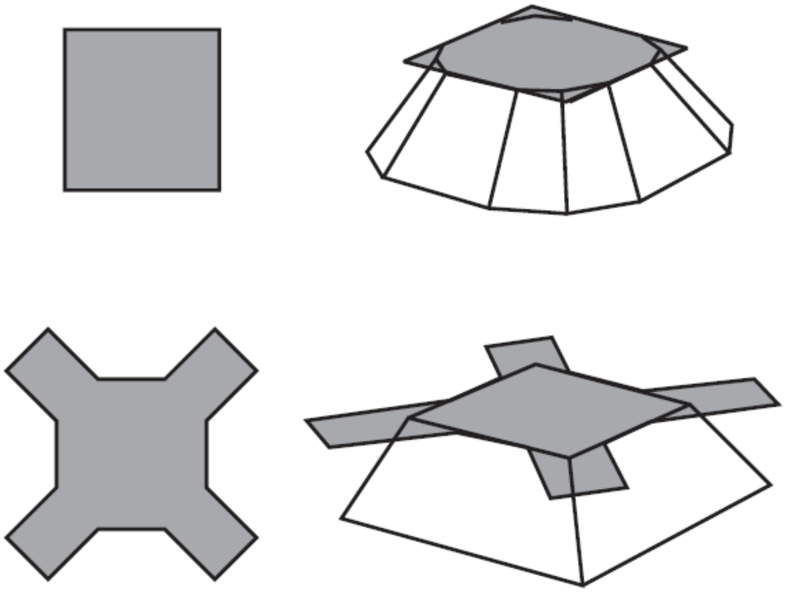
Etching Profile



[100]-oriented wafers

[110]-oriented wafer

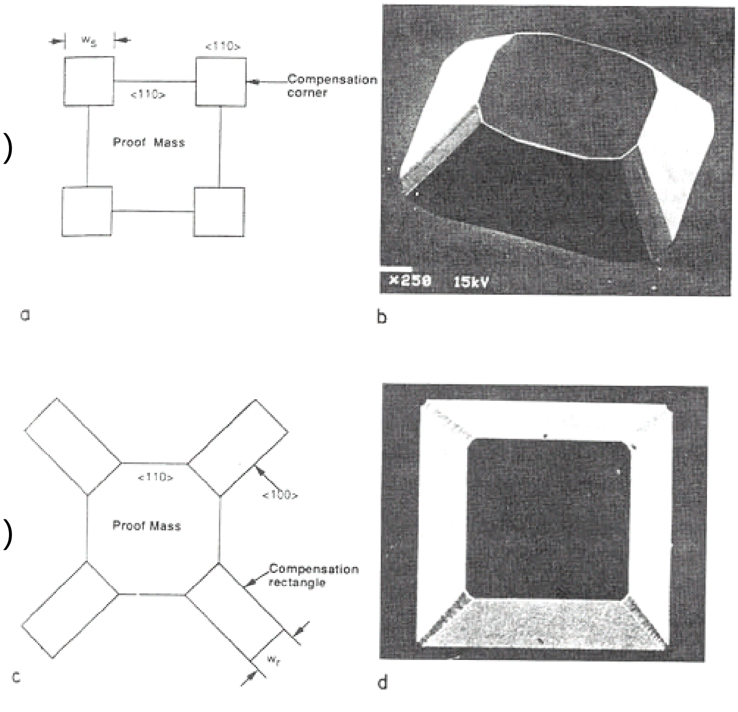
Corner Compensation



Corner Compensation

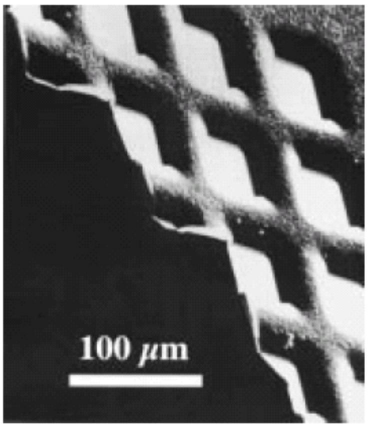
EDP
(100) > (110) > (111)

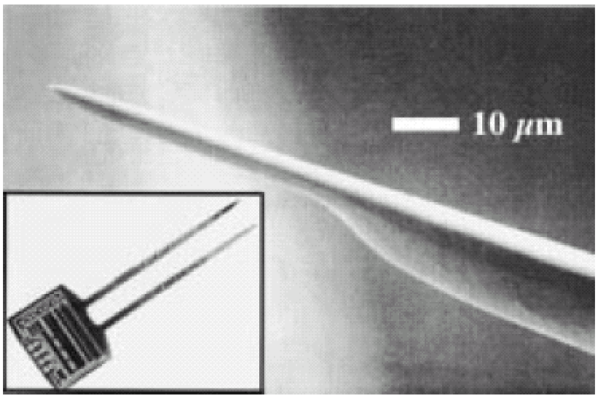
KOH
(110) > (100) > (111)



Etch-Rate Modulation

- Highly p-doped silicon regions greatly attenuate the etch rate
- Selective doping can be used to define specific regions of the silicon that remain, while the bulk is etched away



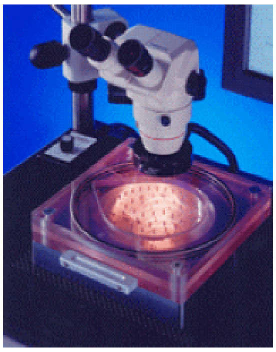


Vapor Phase Etching of Silicon

- Vapor-phase etchant XeF_2

$$2XeF_{2(v)} + Si_{(s)} \rightarrow 2Xe_{(v)} + SiF_{4(v)}$$

  - Set-up
    - Xe sublimes at room T
    - Closed chamber, 1-4 Torr
    - Pulsed to control exothermic heat of reaction
  - Etch rates: 1-3 µm/min (up to 40), isotropic
  - Etch masks: photoresist, SiO_2, Si_3N_4, Al, metals
  - Issues
    - Etched surfaces have granular structure, 10 µm roughness
    - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF



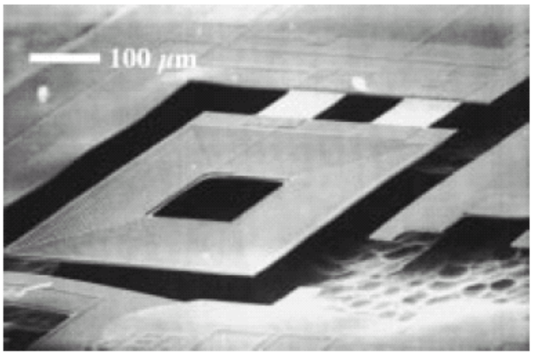
Xactix

Vapor-Phase Etching

- Xenon difluoride etching

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4$$

- Non-plasma, isotropic, and dry
- Very high selectivity for aluminum, silicon dioxide, silicon nitride, and photoresist

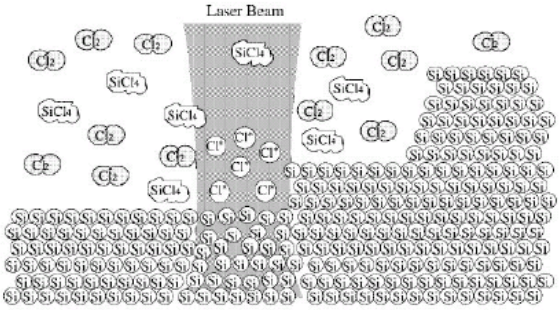


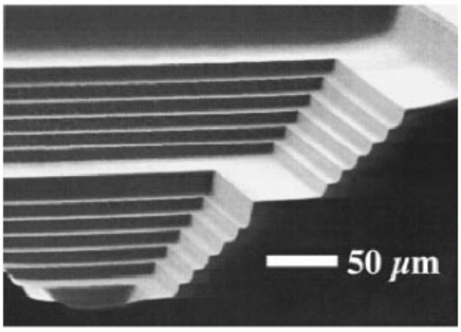
Vapor-Phase Etching

- Interhalogen etch chemistries
  - Avoid the extremely rough silicon surfaces that are formed using XeF_2 etching
  - Thermal silicon dioxide mask and various interhalogen gases (BrF_3 and ClF_3) with a xenon diluent
- Laser-driven vapor-phase etching

Laser-Driven Etching

- Laser-Assisted Chemical Etching
  - Laser creates Cl radicals from Cl_2; Si converts to $SiCl_4$.
  - Etch rate: 100,000 $\mu m^3/s$; 3 min to etch $500 \times 500 \times 125$ μm^3 trench
  - Surface roughness: 30 nm RMS
  - Serial process: patterned directly from CAD file

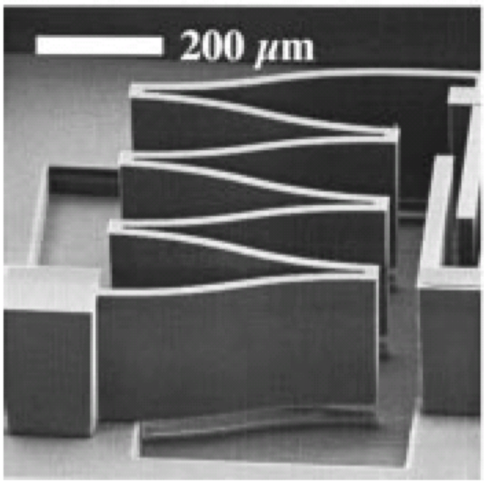


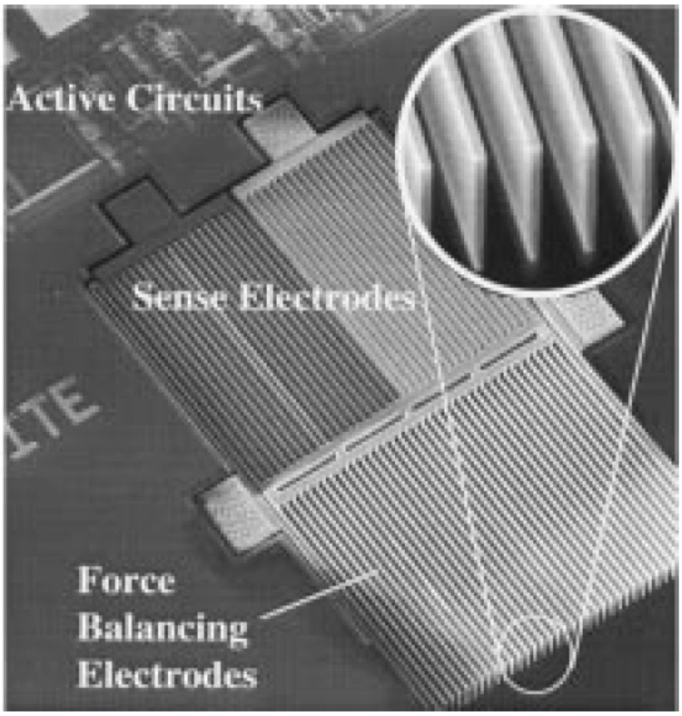


Laser-assisted etching of a 500×500 μm^2 terraced silicon well. Each step is 6 μm deep.

Revise, Inc.

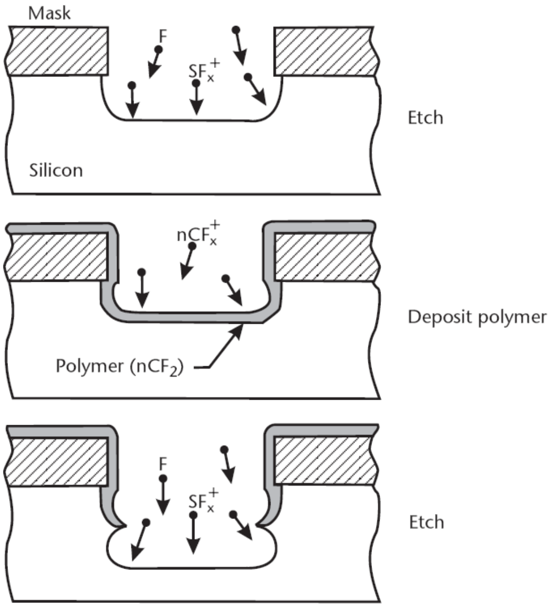
Deep Reactive Ion Etching

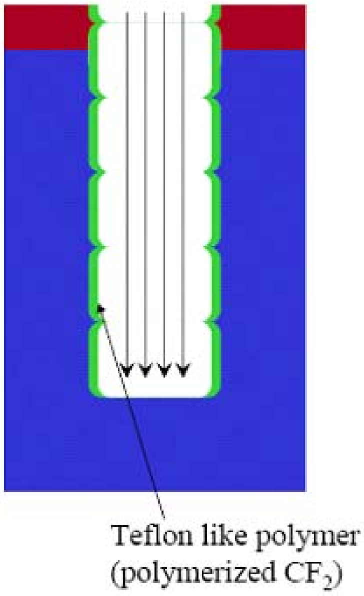




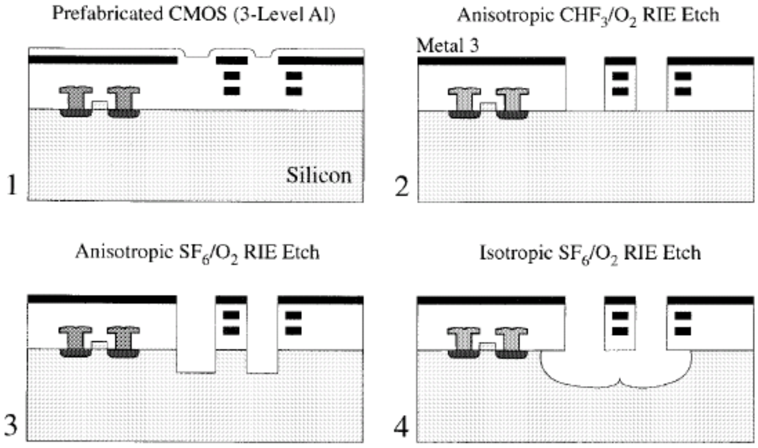
Deep Reactive Ion Etching

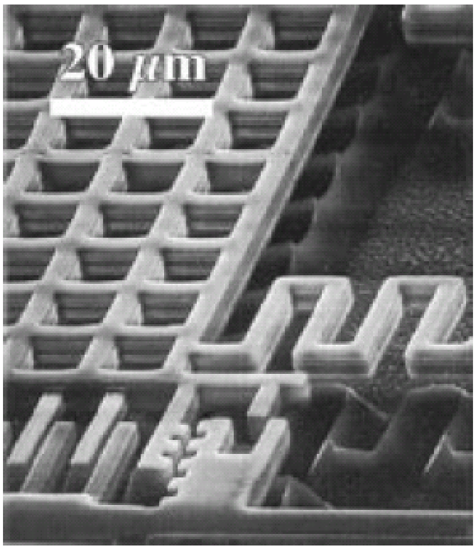
- Alternating between etching and protective polymer deposition





CMOS Integration





Problem 6 – Etching (21%)

The (100) wafer shown below has nitride masks on its top and bottom surfaces.

(1) With KOH, the etch selectivity between the {100} and {111} planes is 400:1 (use ∞:1 in your calculation), and the {100} etch rate is 1.4 μm/min.

(2) With TMAH, the etch selectivity between the {100} and {111} planes is 40:1, and the {100} etch rate is 1.2 μm/min.

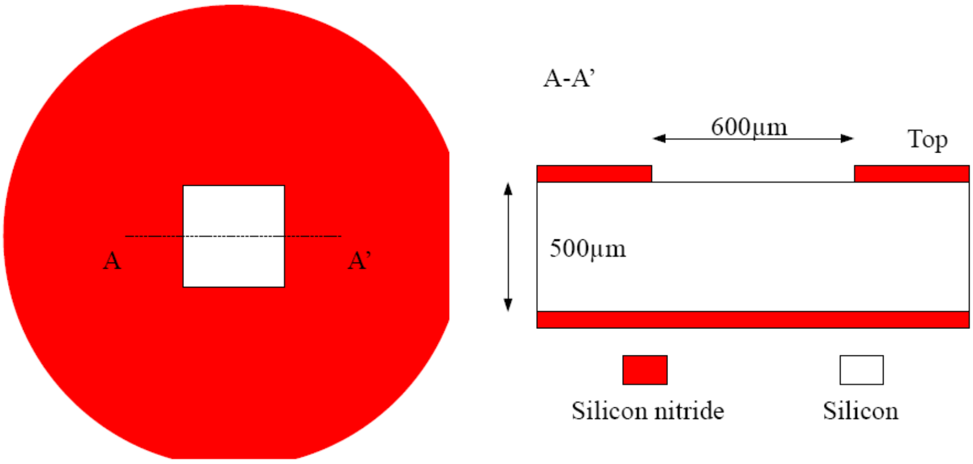
(3) With HNA, the isotropic etch rate is 1 μm/min.

For anisotropic etching, assume that the nitride layers and all other silicon crystal planes are not etched. Sketch the wafer cross sections after 200 minutes of etching (3%) and determine the following dimensions after etching in the all three cases:

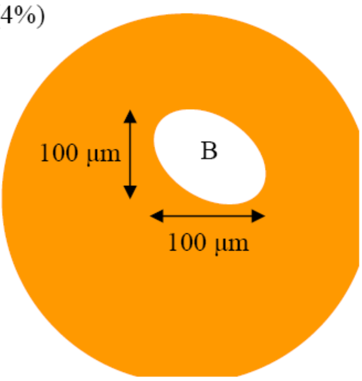
(a) Silicon etch depth (3%)

(b) Silicon etch width at top (6%)

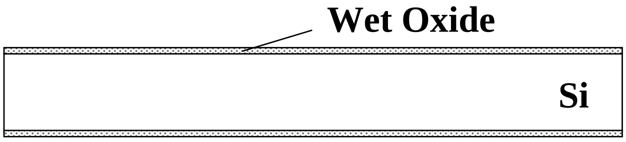
(c) Silicon etch width at bottom (3%)



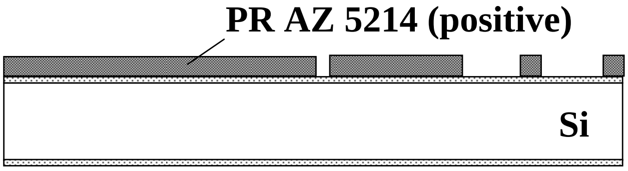
(d) In case there is an elliptic opening B on the top nitride mask, what will be the final shape of the cavity after 200 minutes of KOH etching? (Sketch both the top and cross-sectional views.) (4%)



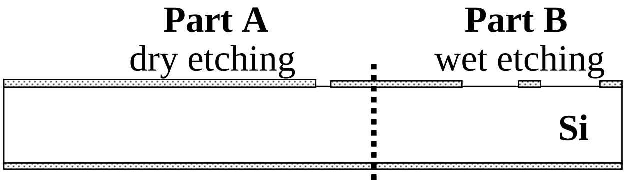
Lab 1 and 2



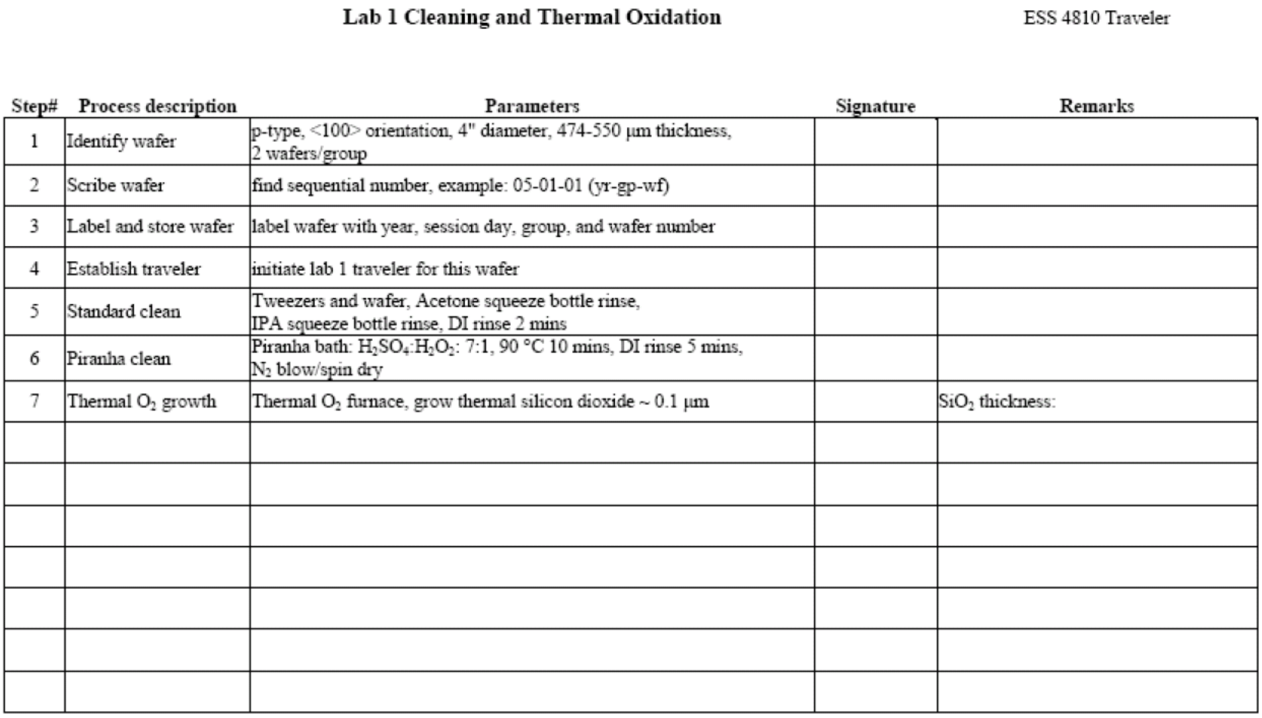
Lab 1:
1. Wafer cleaning
2. Thermal oxidation



Lab 2-1:
1. Lithography
(PR AZ 5214, mask #1
for bulk etching window)



Lab 2-2:
1. Break wafer into A and B
2. B: BOE wet etching
A: RIE dry etching
3. PR strip, wafer cleaning



Lab 1 Cleaning and Thermal Oxidation ESS 4810 Traveler

Step#	Process description	Parameters	Signature	Remarks
1	Identify wafer	p-type, <100> orientation, 4" diameter, 474-550 µm thickness, 2 wafers/group		
2	Scribe wafer	find sequential number, example: 05-01-01 (yr-gp-wf)		
3	Label and store wafer	label wafer with year, session day, group, and wafer number		
4	Establish traveler	initiate lab 1 traveler for this wafer		
5	Standard clean	Tweezers and wafer, Acetone squeeze bottle rinse, IPA squeeze bottle rinse, DI rinse 2 mins		
6	Piranha clean	Piranha bath: H_2SO_4:H_2O_2: 7:1, 90 °C 10 mins, DI rinse 5 mins, N_2 blow/spin dry		
7	Thermal O_2 growth	Thermal O_2 furnace, grow thermal silicon dioxide ~ 0.1 µm		SiO_2 thickness:

Lab 2 Lithography and Wet Etching

ESS 4810 Traveler

Step#	Process description	Parameters	Signature	Remarks
8	Standard clean	Tweezers and wafer, Acetone squeeze bottle rinse, IPA squeeze bottle rinse, DI rinse 2 mins		
9	Piranha clean	Piranha bath: H_2SO_4:H_2O_2: 7:1, 90 °C 10 mins, DI rinse 5 mins, N_2 blow/spin dry		
10	DI rinse and air dry	DI rinse for at lease 5 mins and air shower dry		
11	Dehydration bake	120 °C hotplate, 5 mins		
12	HMDS vapor coating	place wafer into beaker containing ~ 10 ml HMDS (clear chemical) for 5 mins		
13	Wafer prespin	check wafer spin rate, time, set up for 3000 rpm and 30 seconds		
14	AZ 5214-EIR coat	dark chemical, 3000 rpm and 30 seconds for spinner, 1 full dropper, spin quickly		
15	Prebake photoresist	100 °C hotplate, 1 min, center of hotplate		Temp of hotplate:
16	Mask alignment	roughly align mask with wafer flat, exposure for $50mJ/cm^2$, **mask #1**		Exposure time:
17	Development	AZ 400k developer: DI=1:5, approx 1 min, DI rinse 3 mins, N_2 blow/spin dry		Development time:
18	Microscope inspection	inspect for good image transfer, alignment marks, exposure quality marks, TA check		Alignment quality: Exposure quality:
19	Protect finger part	paint PR5214 onto square area for finger pattern		
20	Hard bake	120 °C hotplate, 2 mins		
21	Back side protection	paint wafer back side with PR AZ 5214		PR thickness:
22	Break wafer	break wafers into part A: surface micromachining, part B: bulk micromachining		
	Process for Part B:			
23	BOE preparation	preparation 6:1 BOE (Buffered Oxide Etchant) for open 1 μm SiO2 windows		
24	Wet BOE etching	etching rate ~ 0.08-0.1 μm/min for wet oxide, need ~ 14 mins for 1 μm, hydrophobic		Etching time:
25	PR prestrip	acetone strip PR, IPA rinse, DI rinse		
26	Piranha clean	Piranha bath: H_2SO_4:H_2O_2: 7:1, 90 °C 10 mins, DI rinse 5 mins, N_2 blow/spin dry		take pictures